

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Adrian P. Wise

Filed: HEREWITH

For: MULTISTANDARD VIDEO
DECODER AND DECOMPRESSION
SYSTEM FOR PROCESSING
ENCODED BIT STREAMS INCLUDING
STORING DATA AND METHODS
RELATING THERETO

§

§ Application No.: Not Yet Known

§

§ Art Unit: 2783 (anticipated)

§

§ Examiner: Follansbee, J. (anticipated)

§

§ Attorney Docket No.:

§

94100414(EP)USC1X1C1D3 PDDD

§

§

COMMUNICATION - SUBMISSION OF FORMAL DRAWINGS

BOX PATENT APPLICATION

Assistant Commissioner of Patents

Washington DC 20231

Sir:


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Transmitted herewith are 169 formal drawings on 124 sheets.

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Respectfully submitted,

DISCOVISION ASSOCIATES



Richard Stokey
Reg. No. 40,383

Date: 1/29/01

DISCOVISION ASSOCIATES
INTELLECTUAL PROPERTY DEVELOPMENT
P.O. Box 19616
Irvine, California 92623
(949) 660-5006

RS:sd

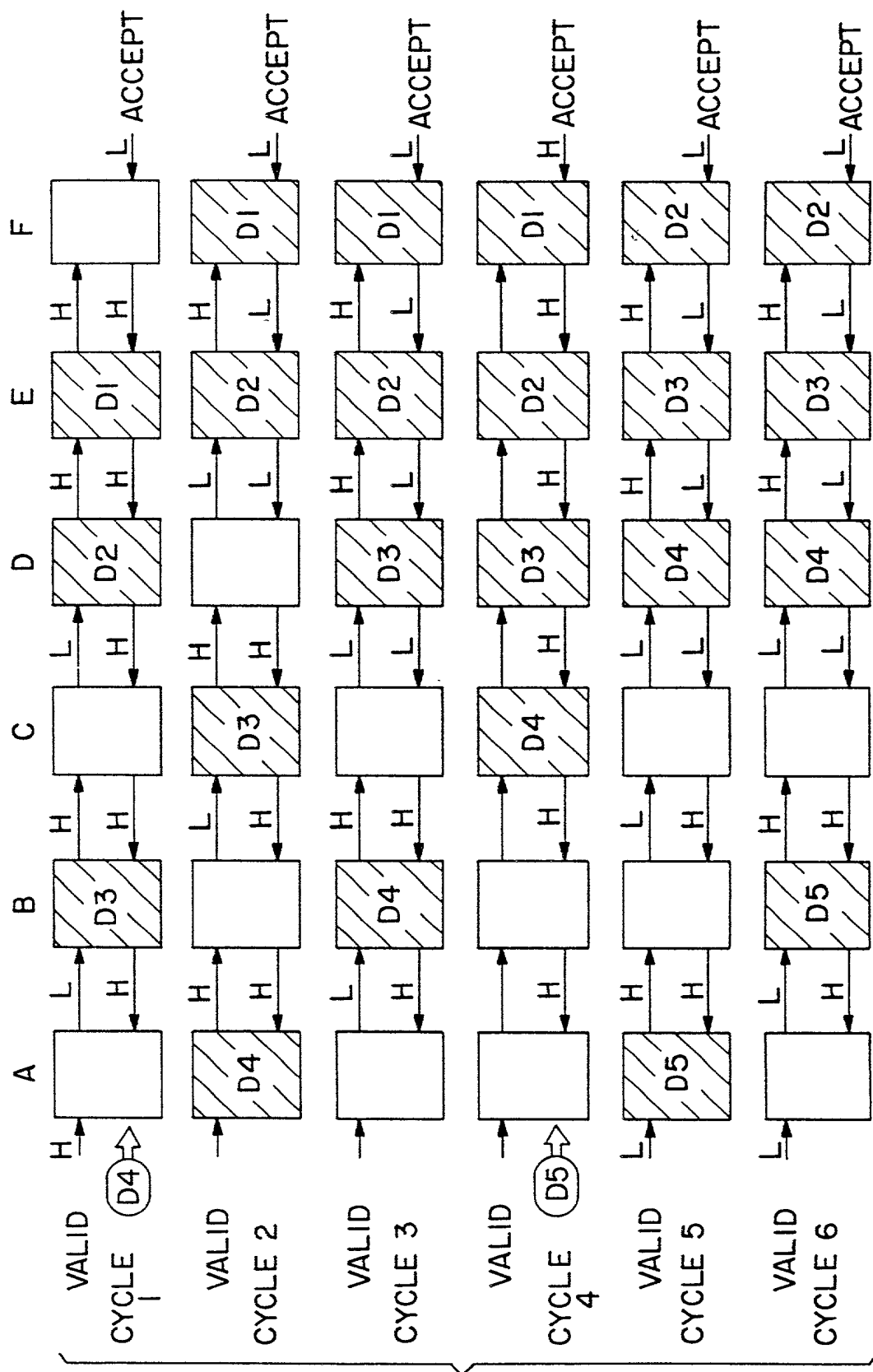


FIG. 1

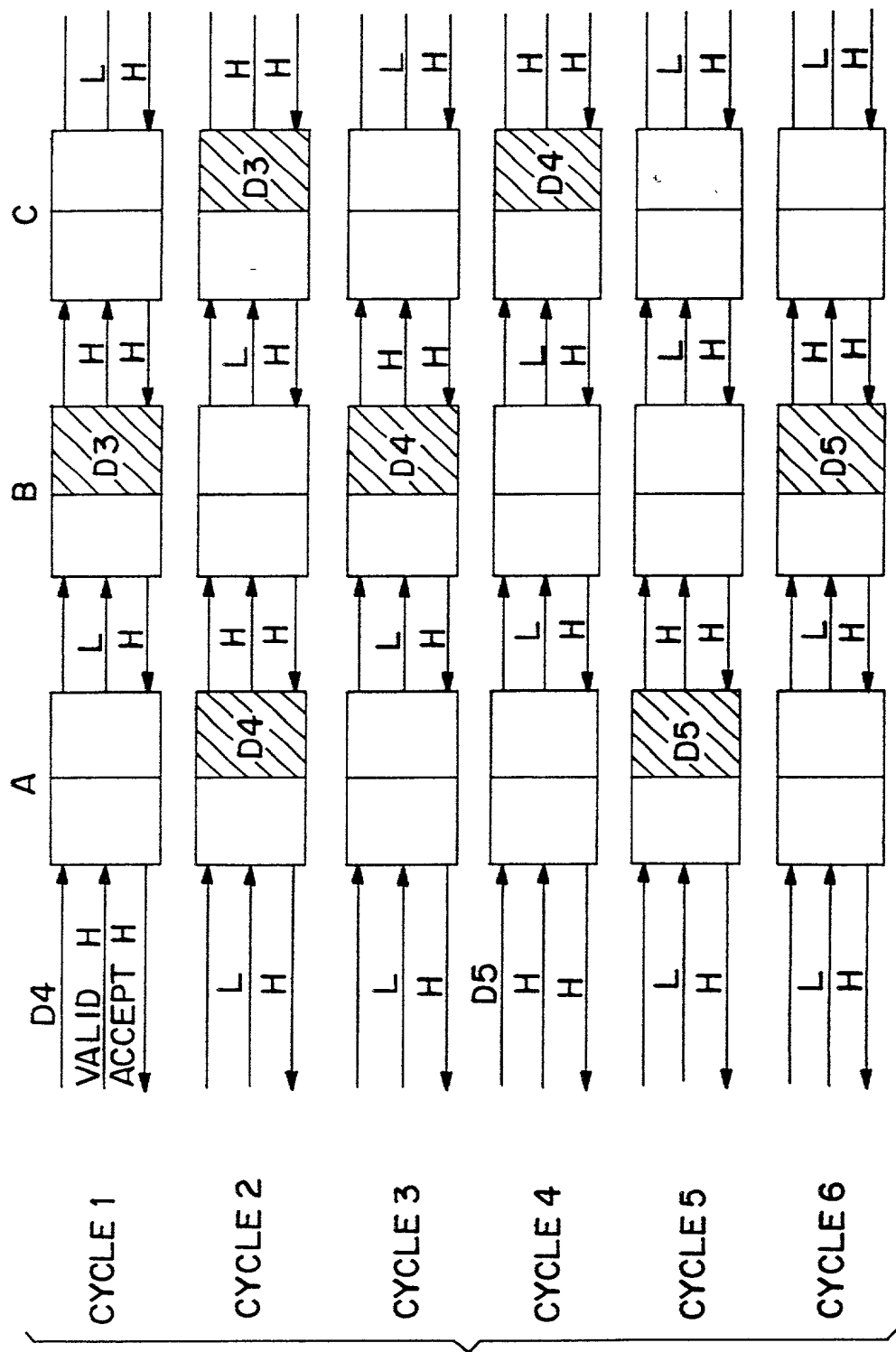


FIG. 2(A)

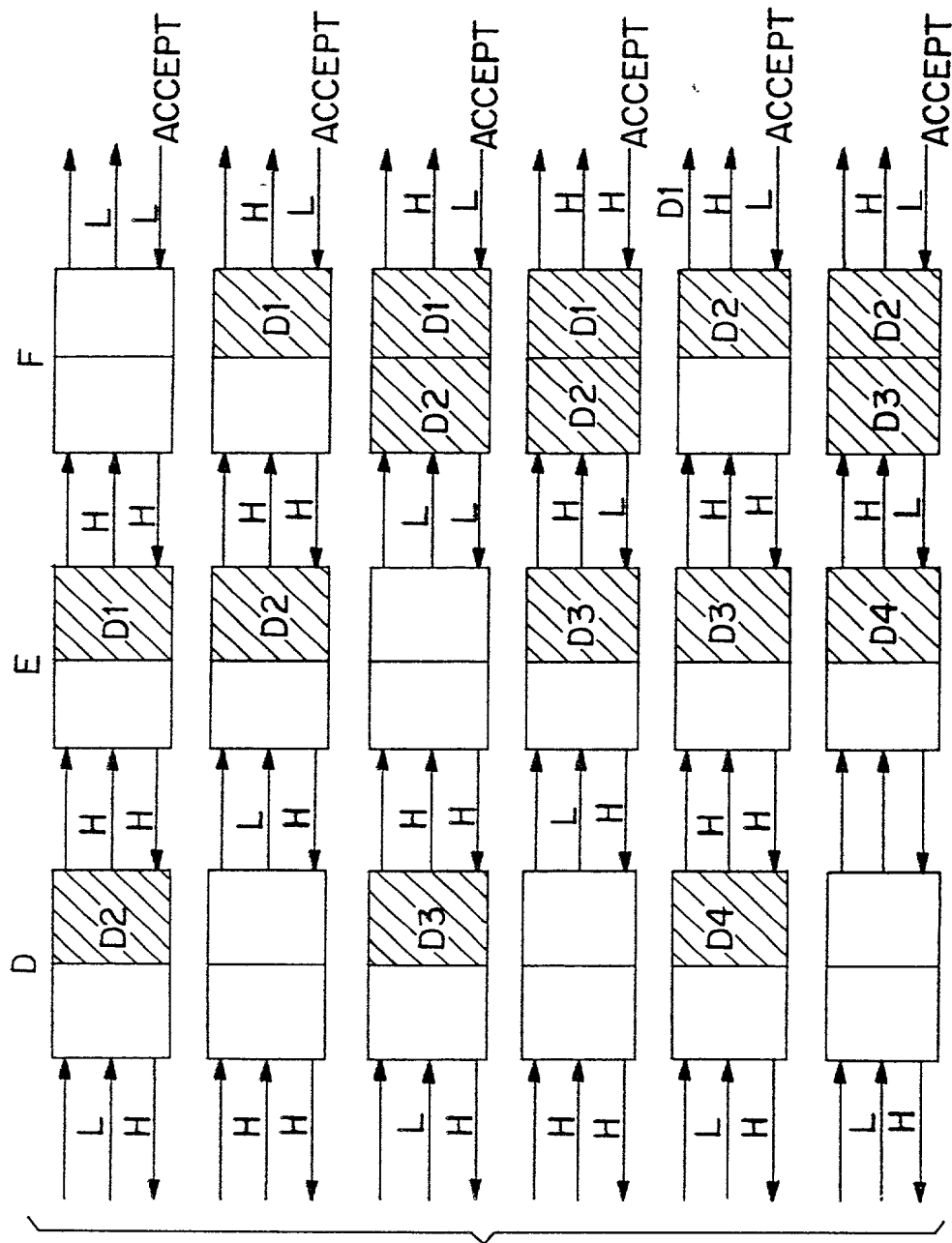
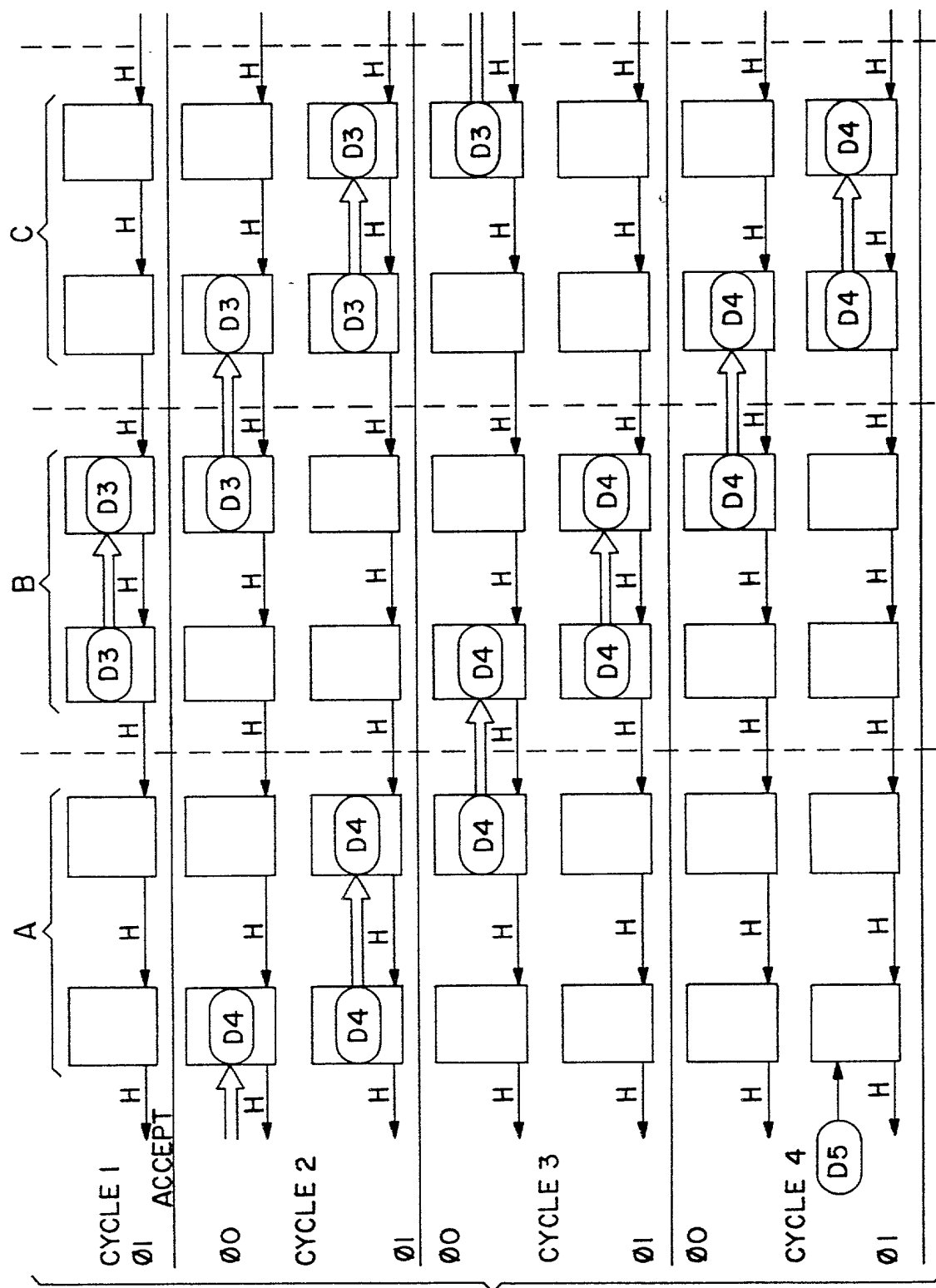
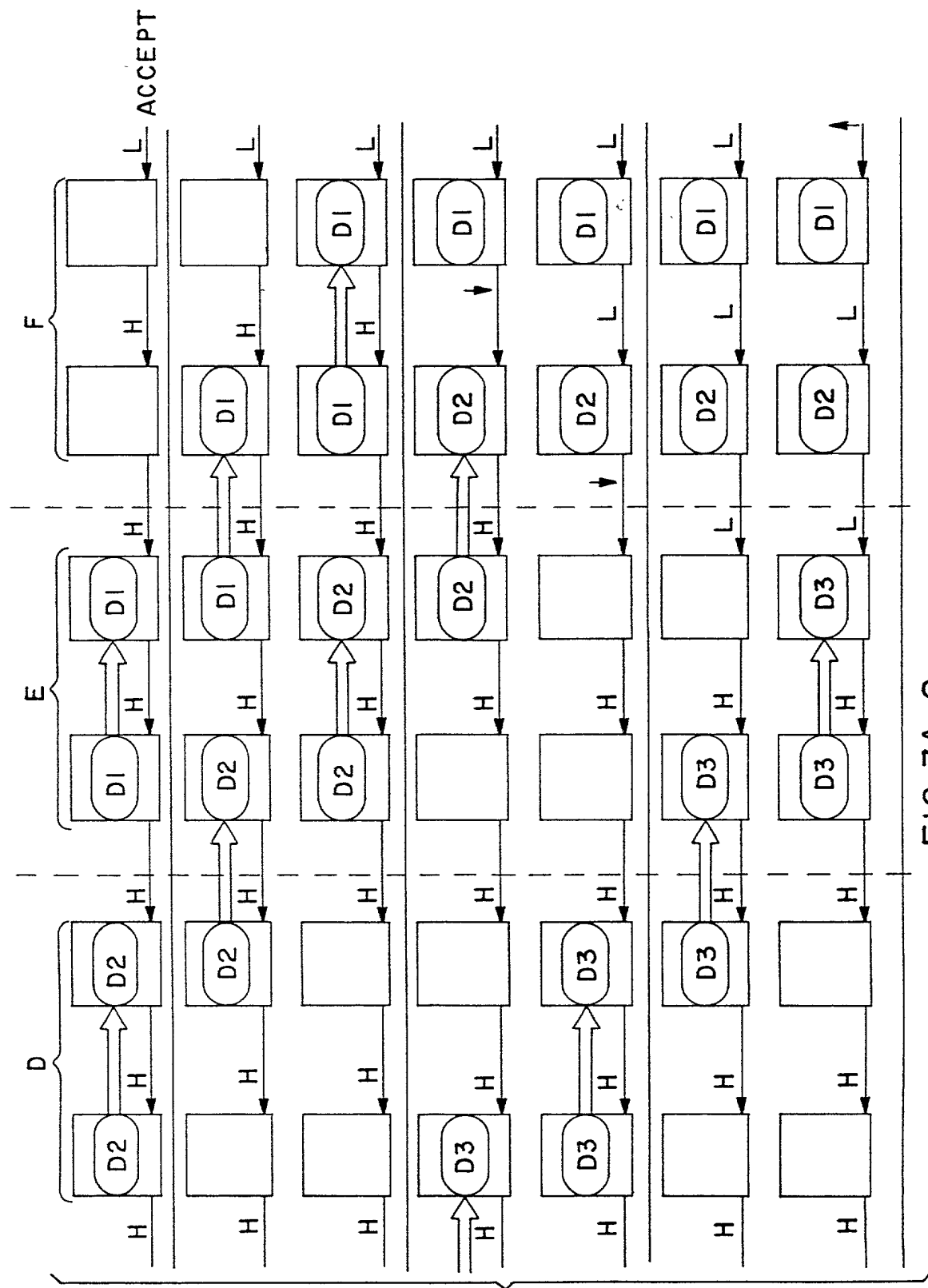


FIG. 2(B)





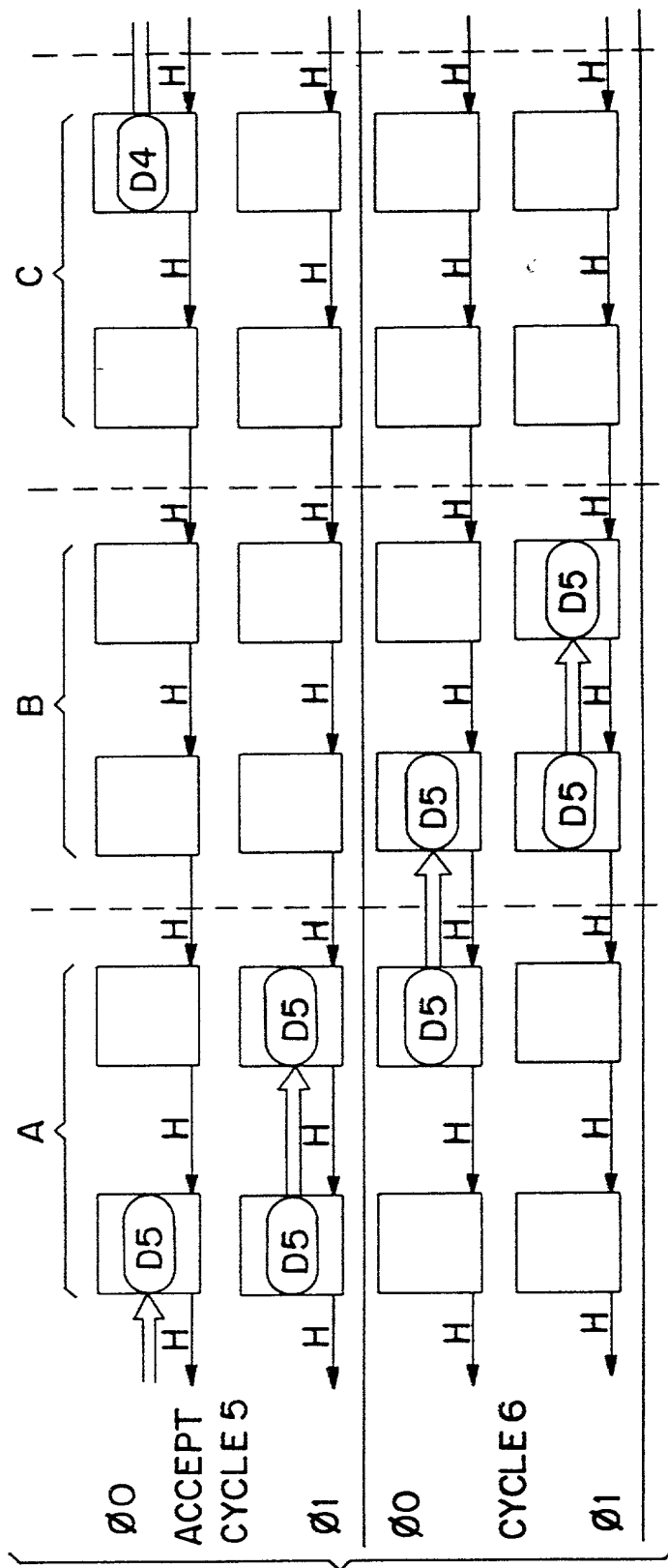


FIG. 3B-I

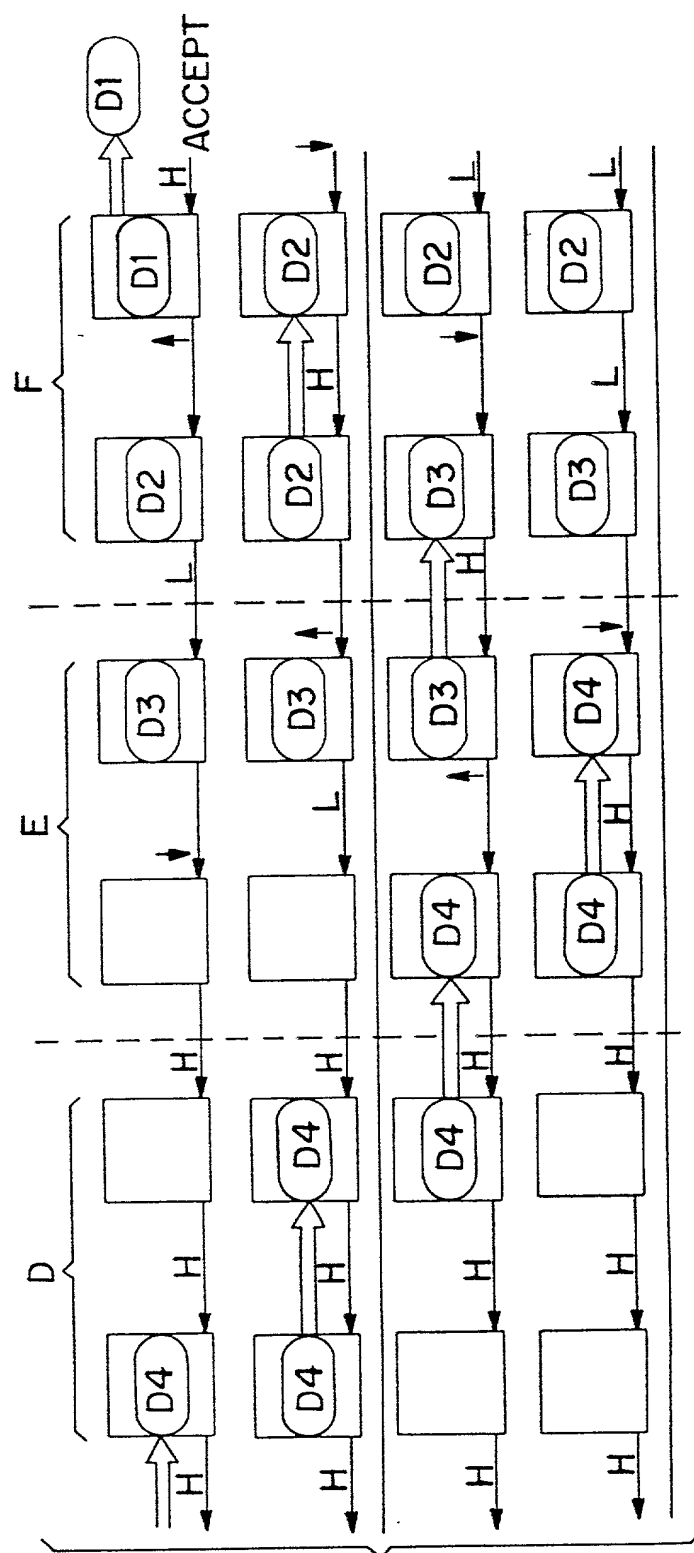


FIG. 3B-2

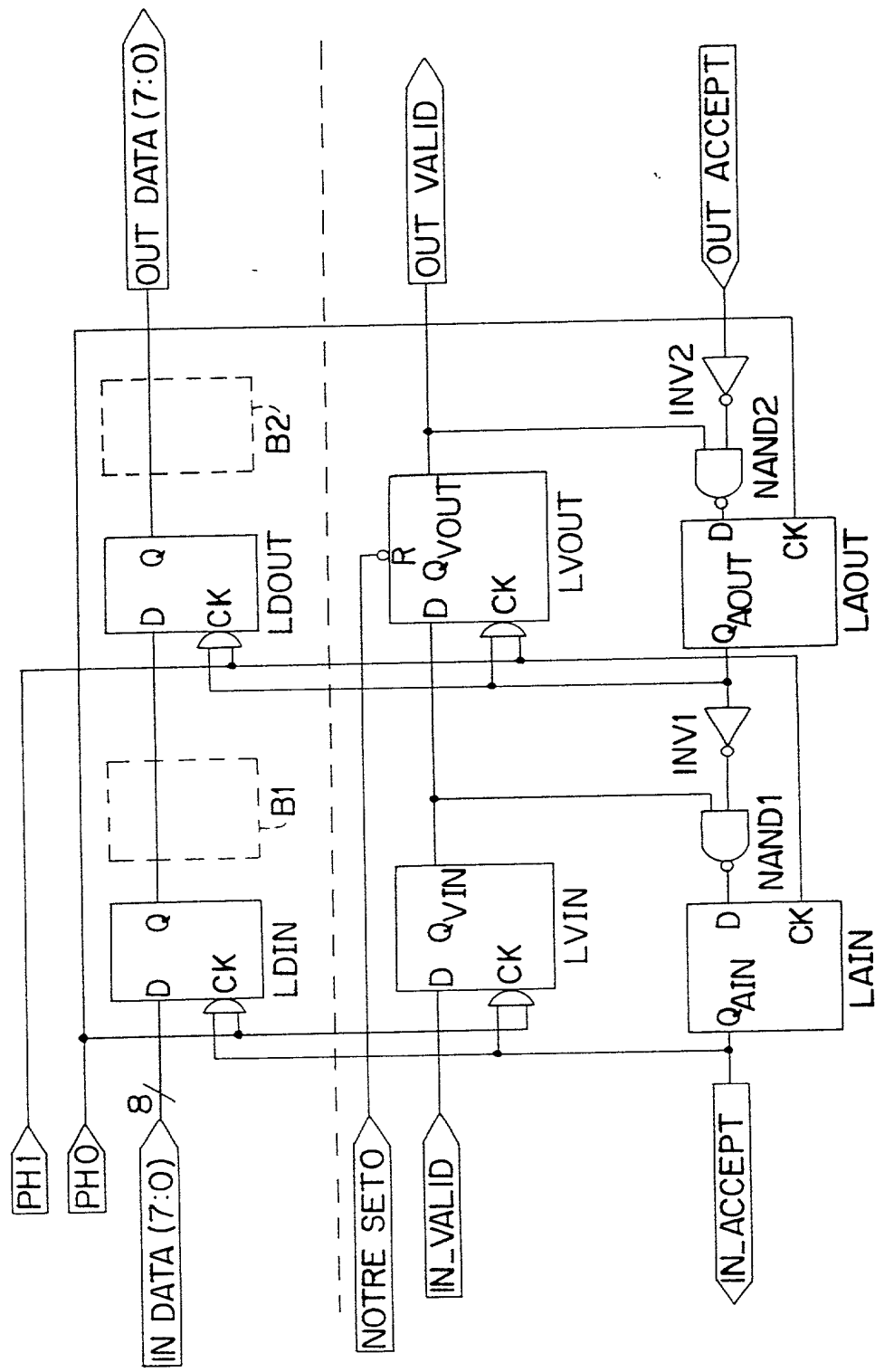


FIG. 4

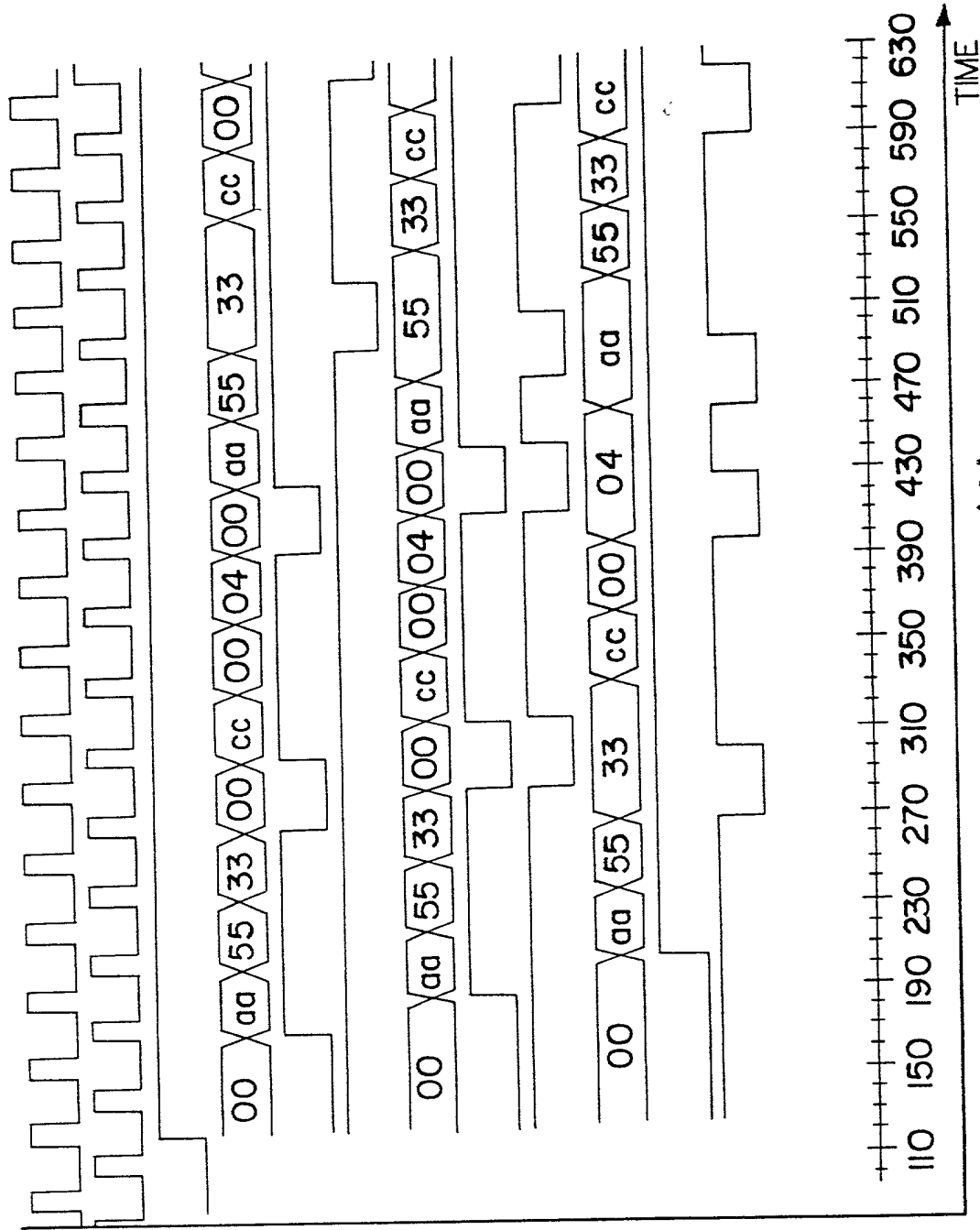


FIG. 5(A)

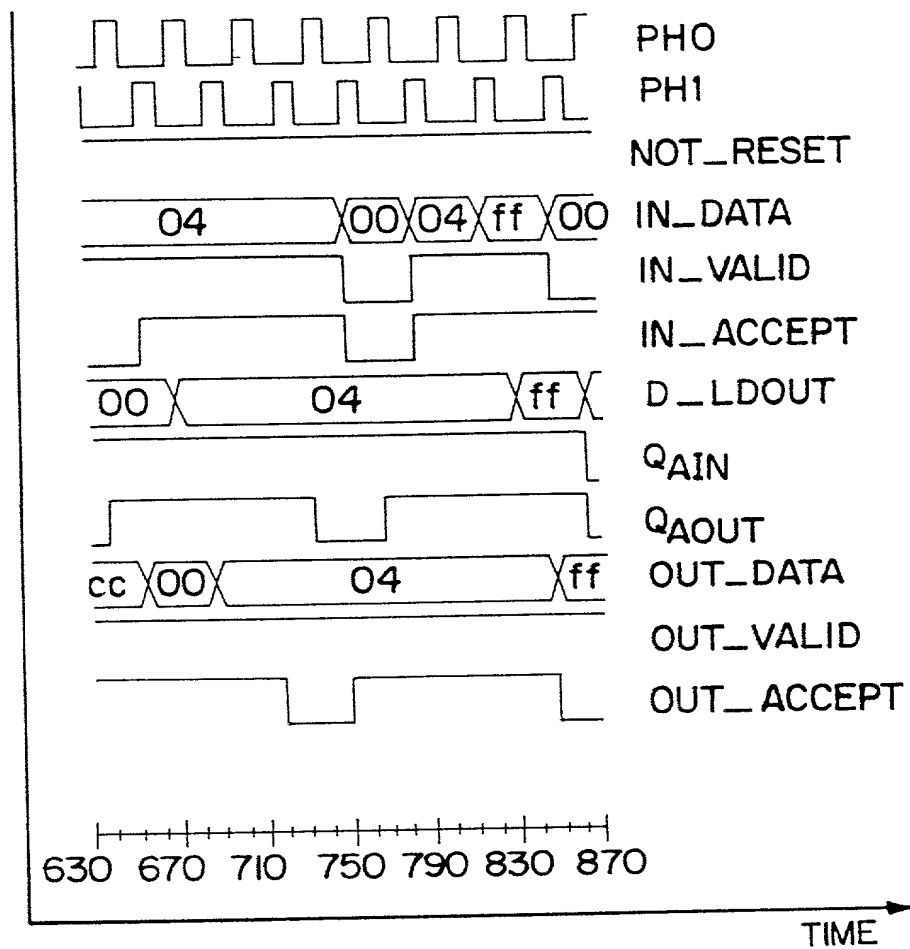


FIG. 5(B)

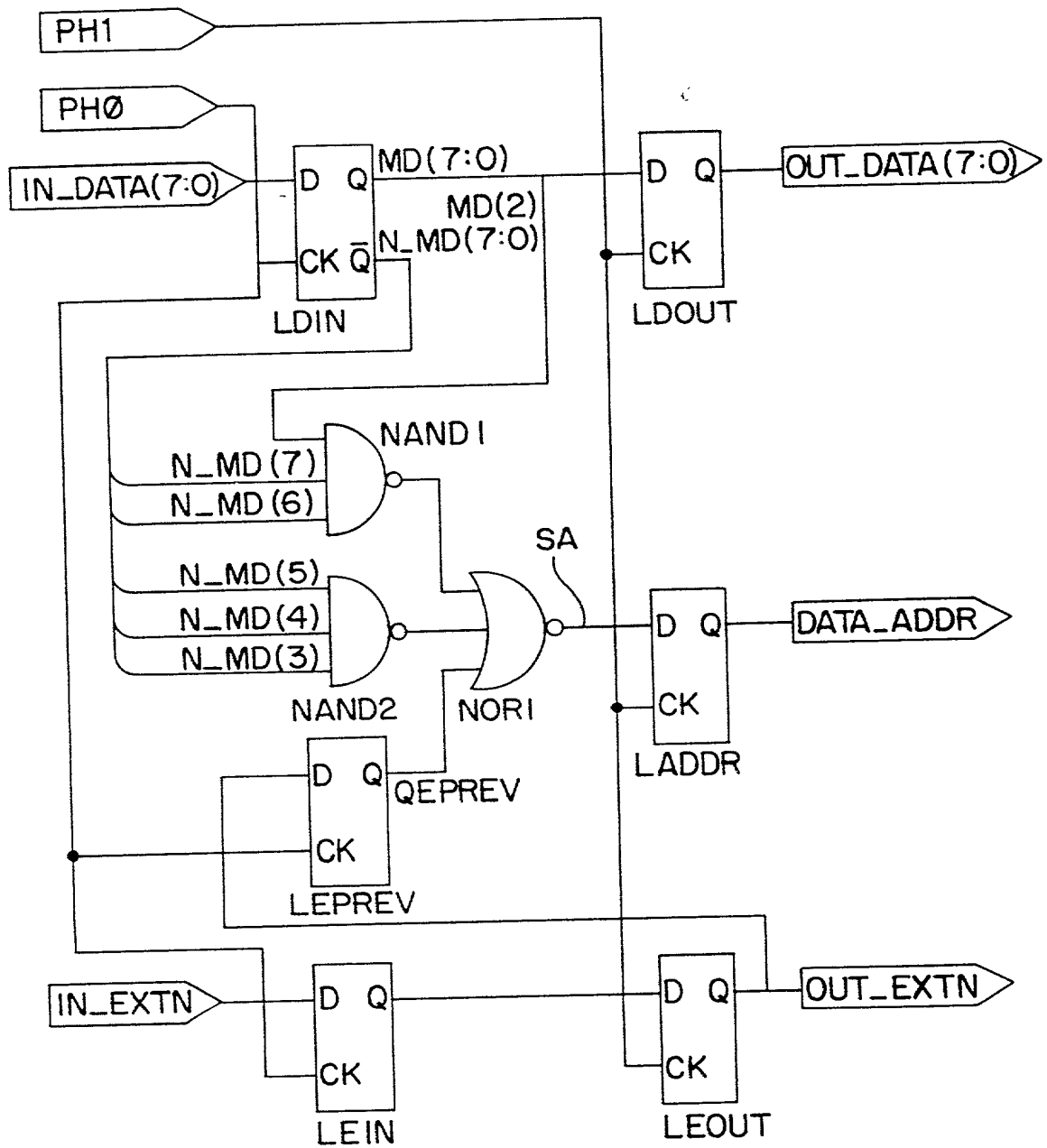


FIG. 6

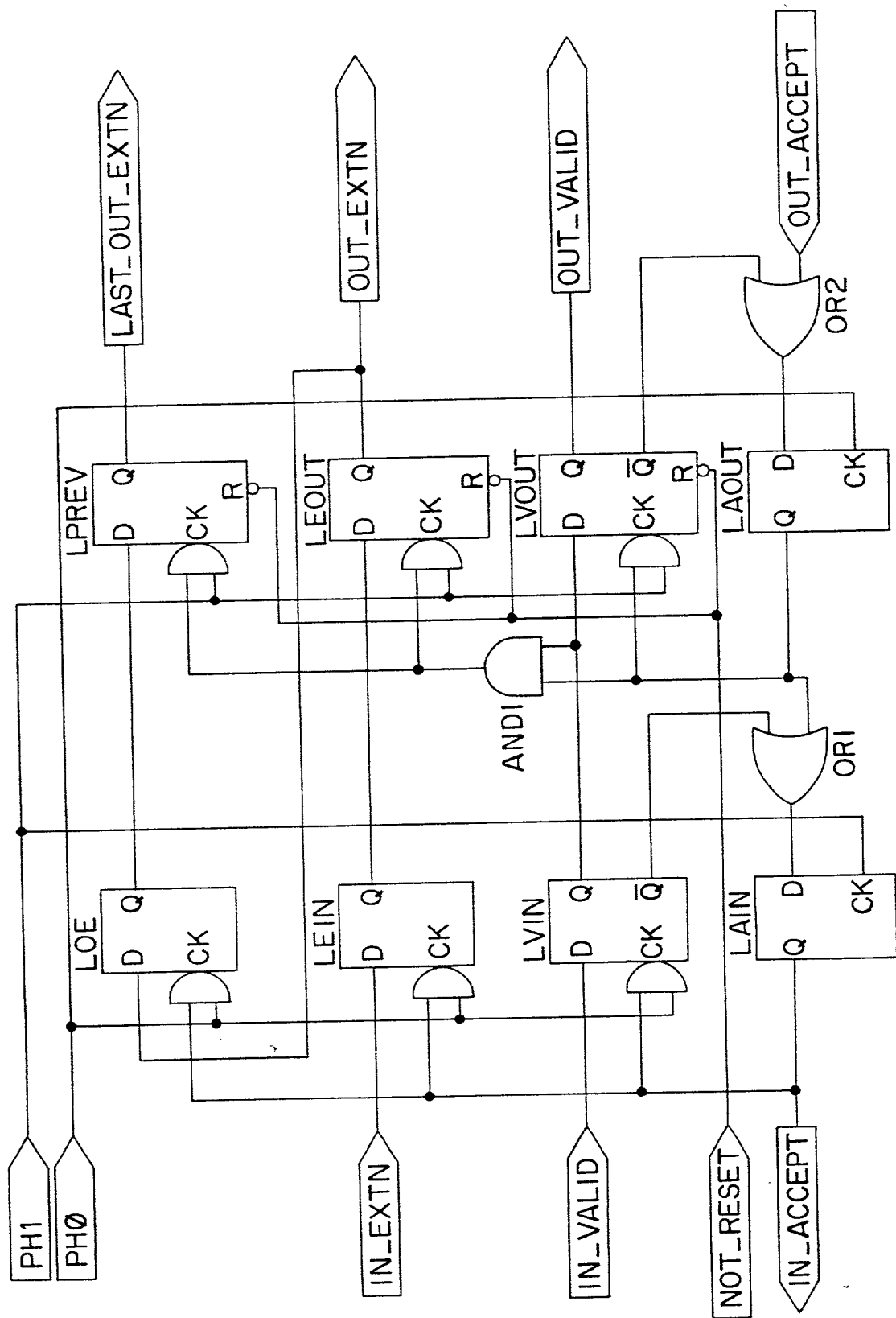


FIG. 7

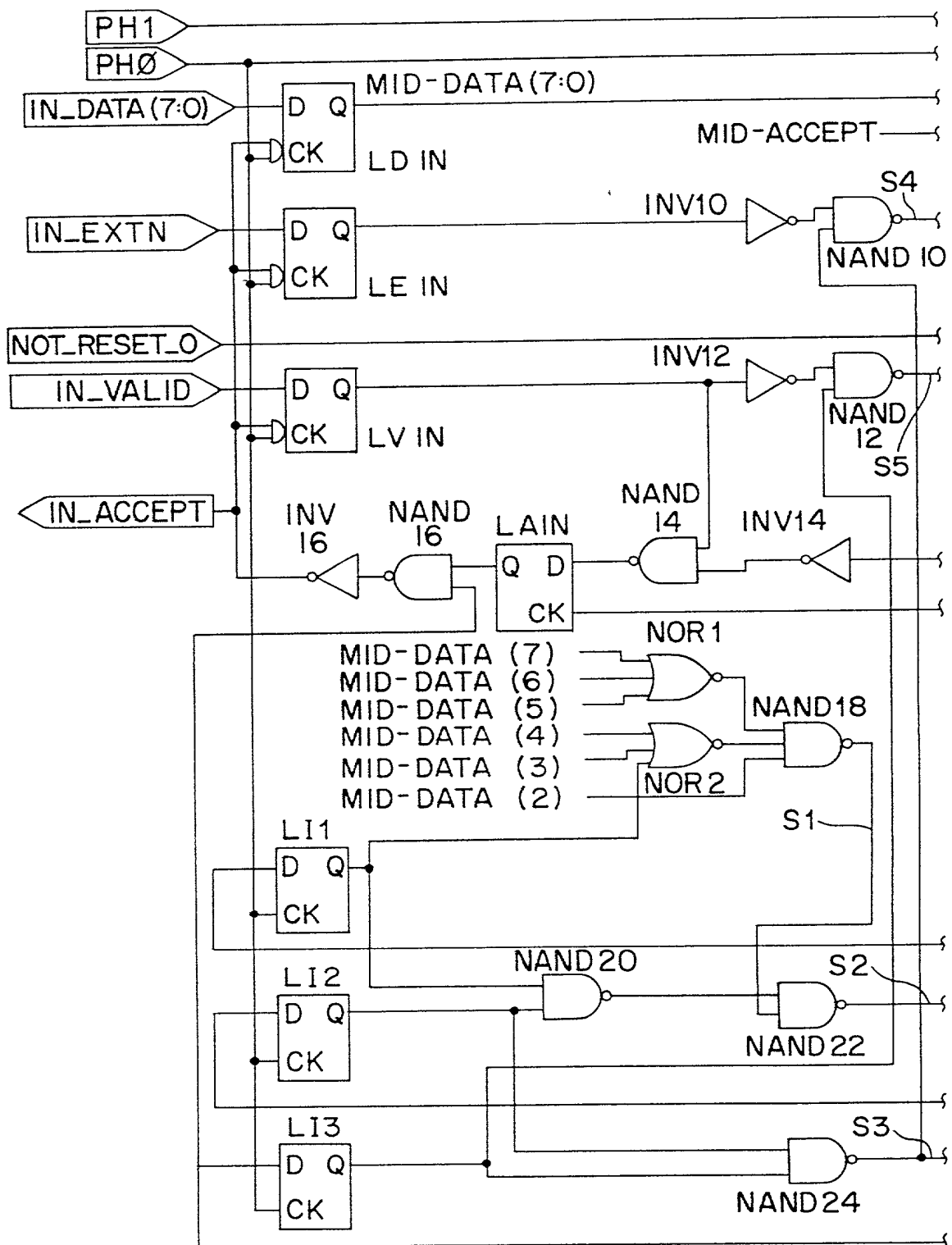


FIG. 8(A)

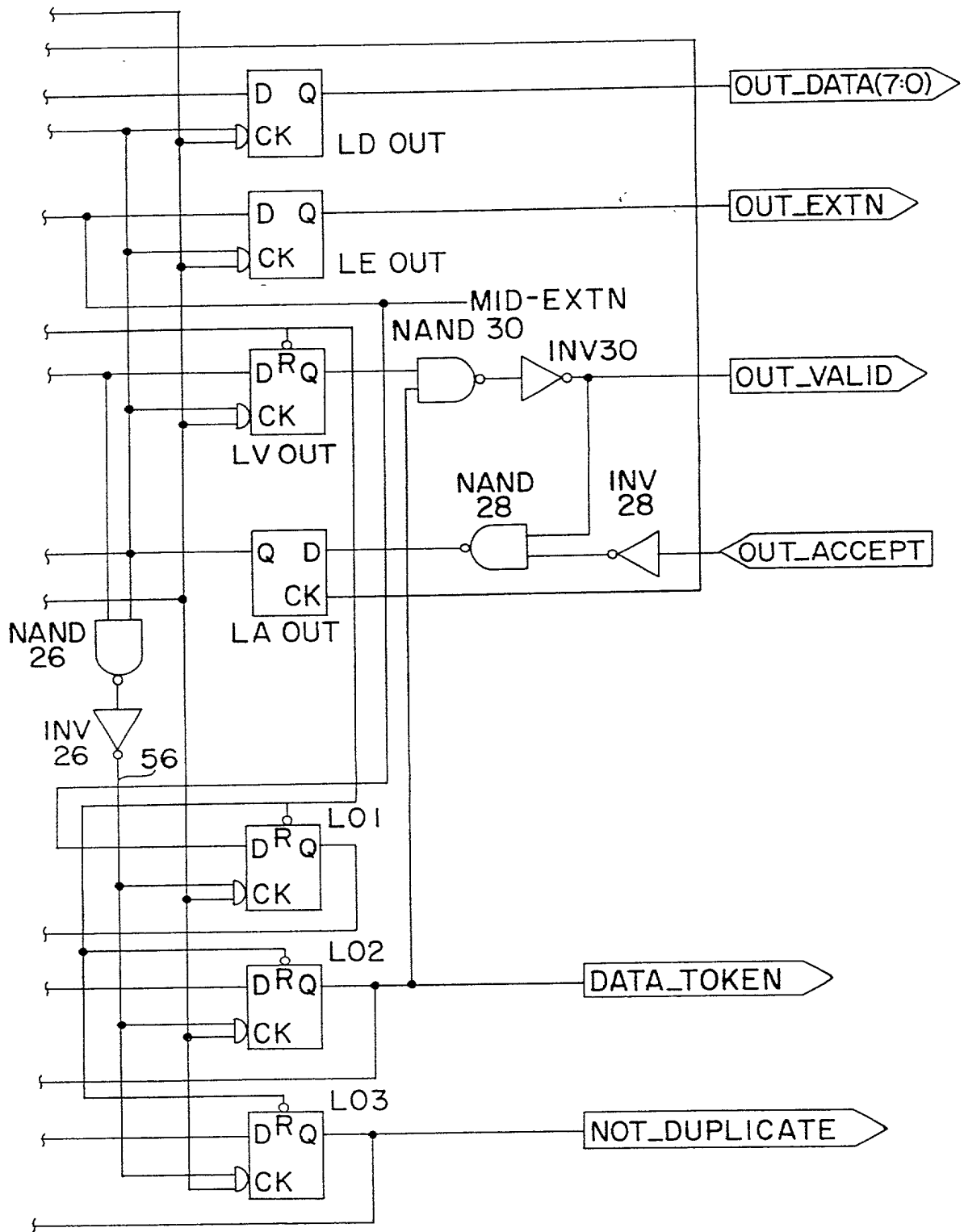


FIG. 8(B)

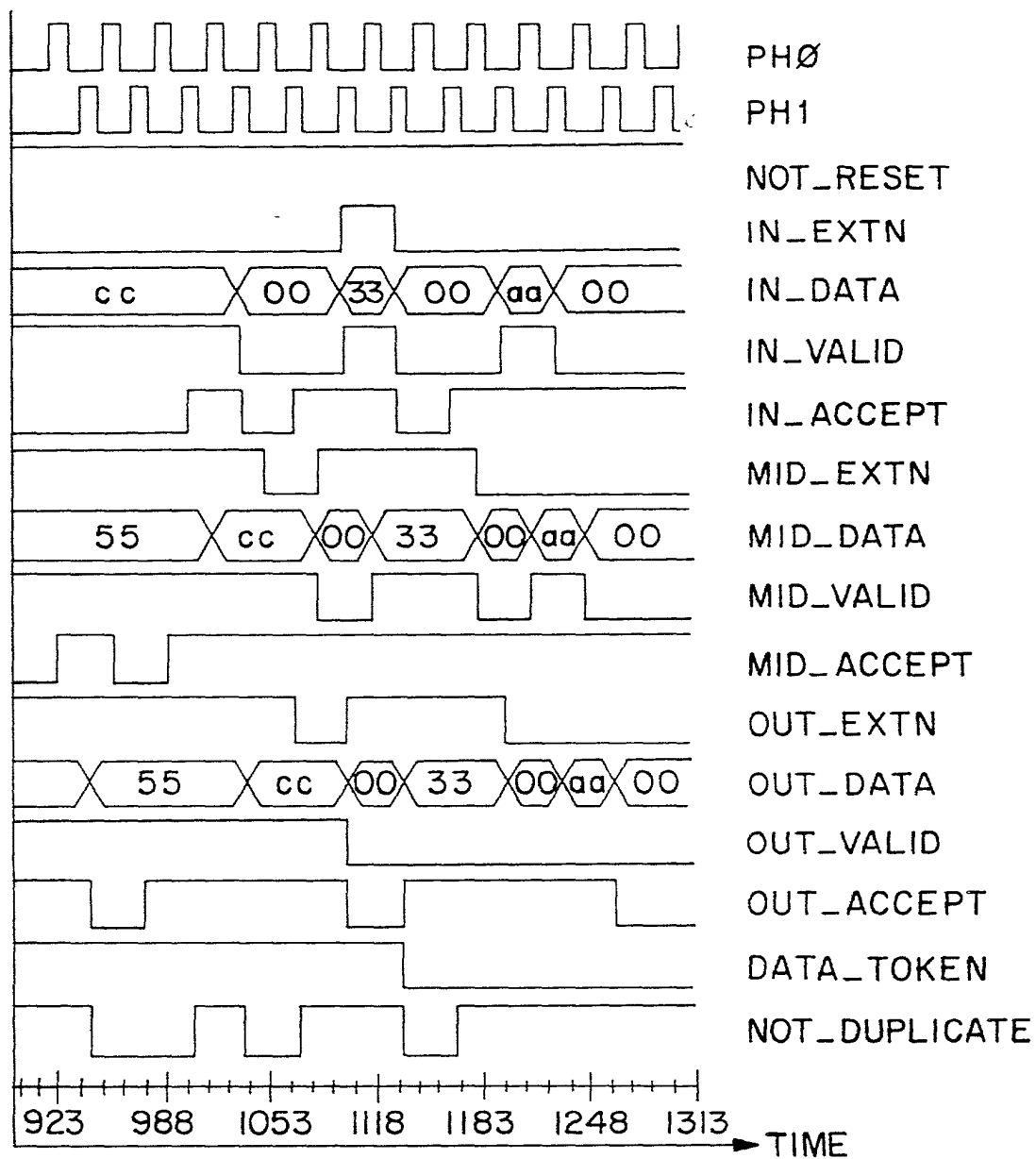


FIG. 9(B)

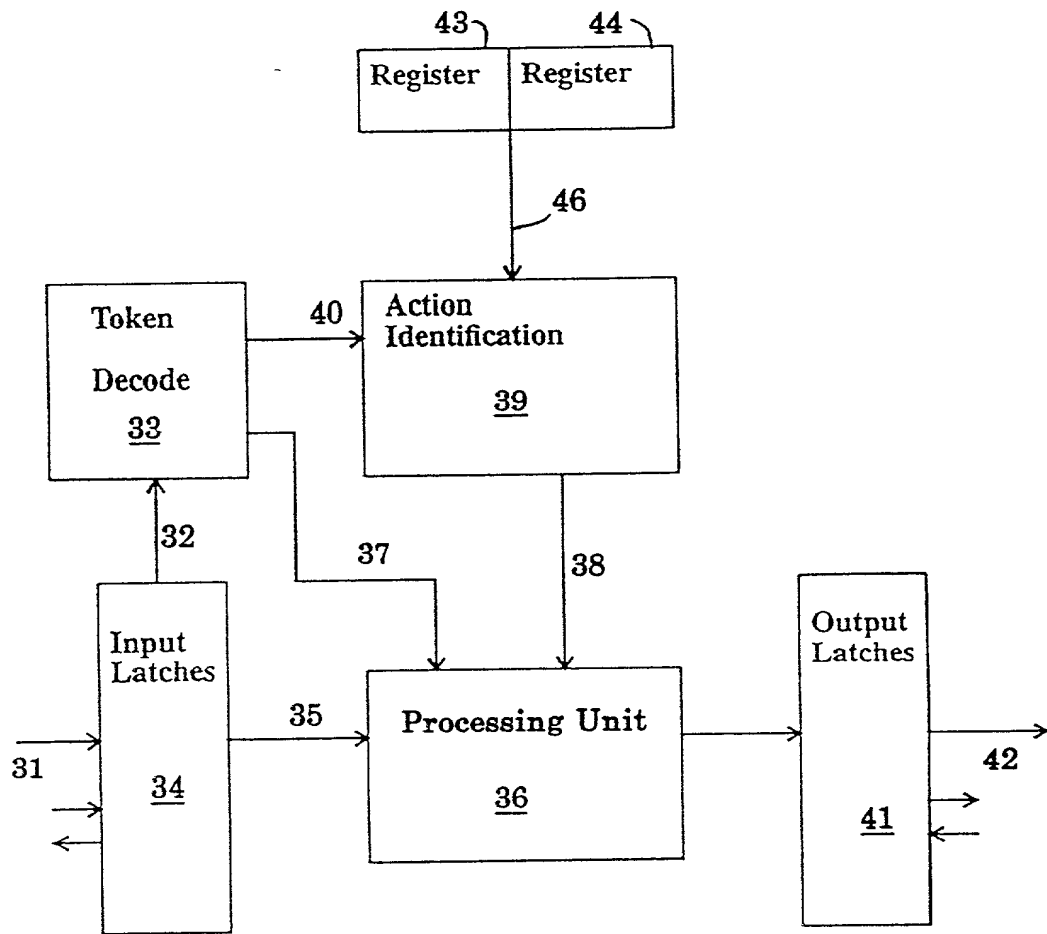


FIG. 10

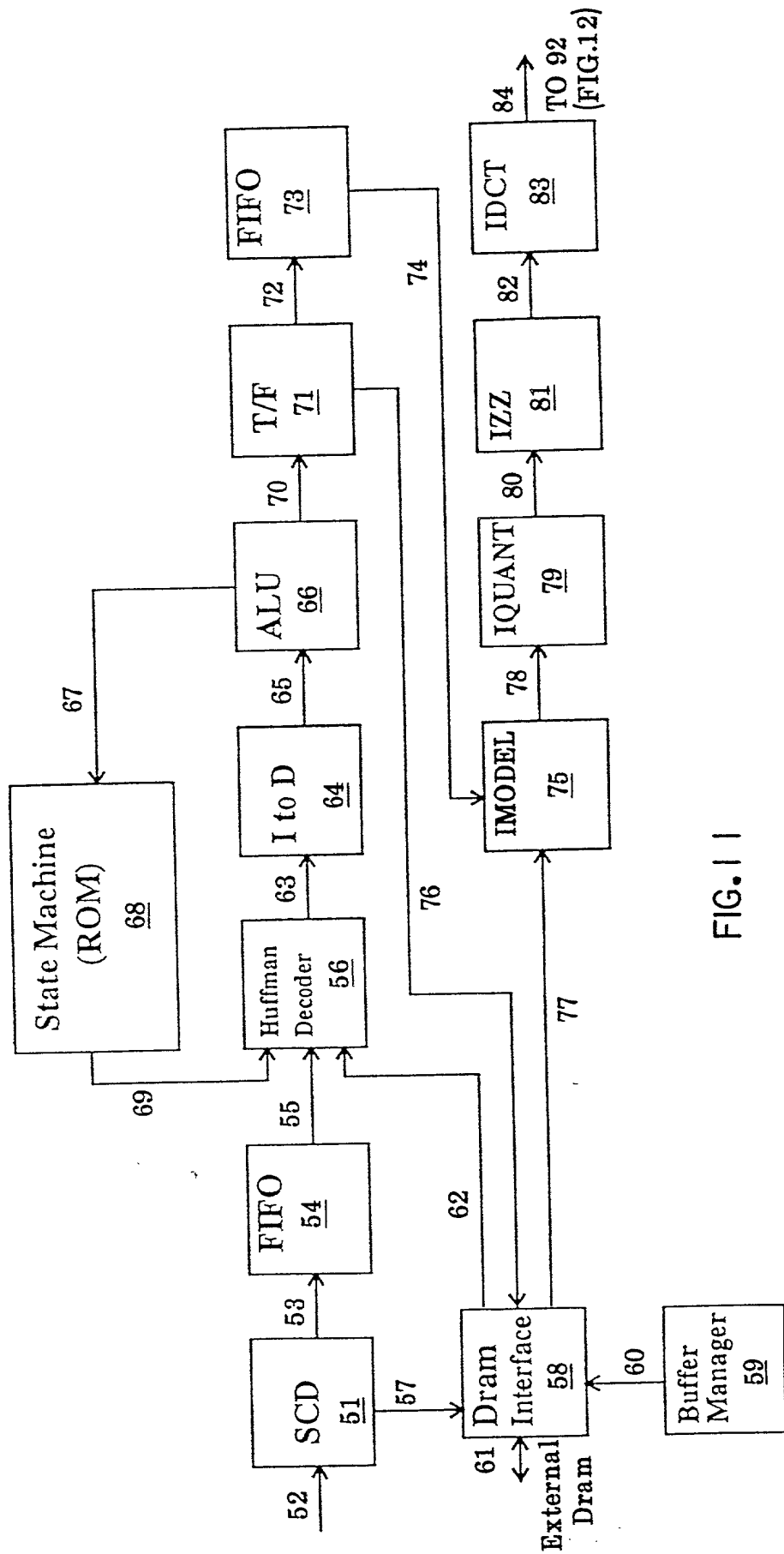


FIG. 11

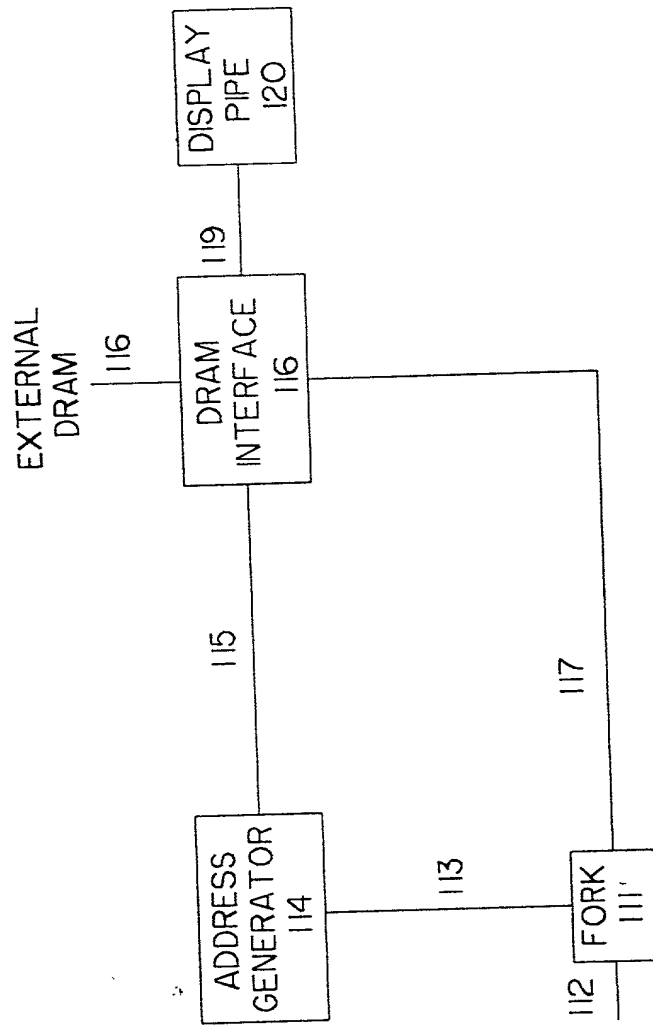
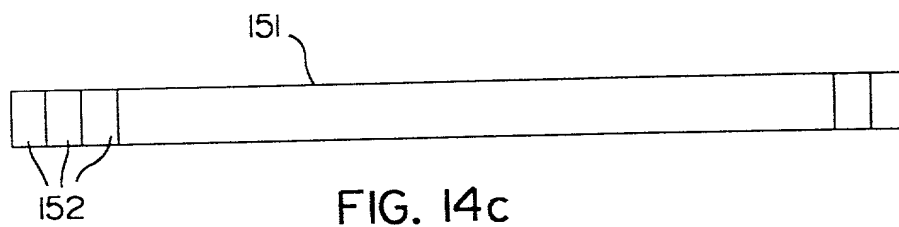
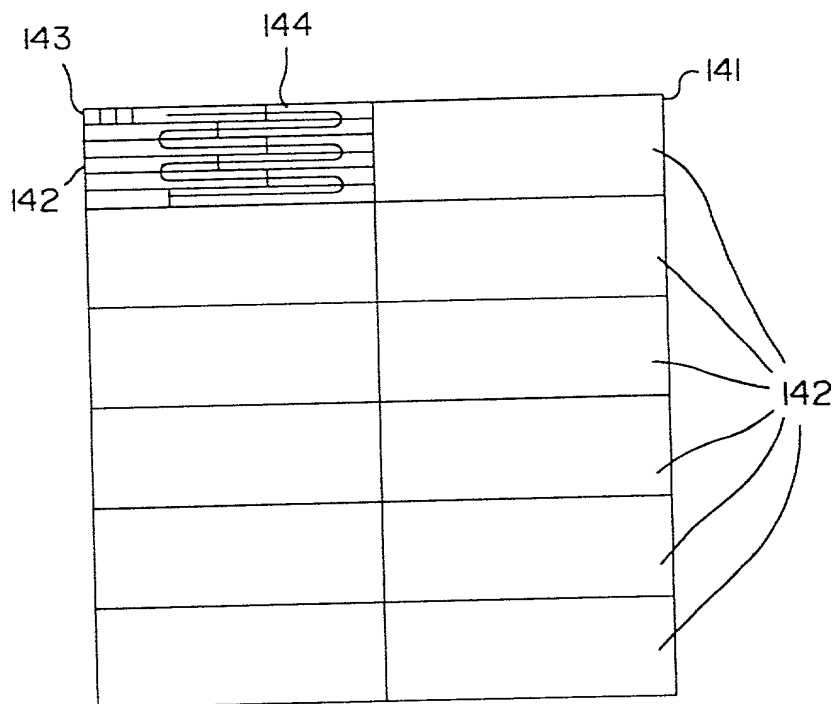
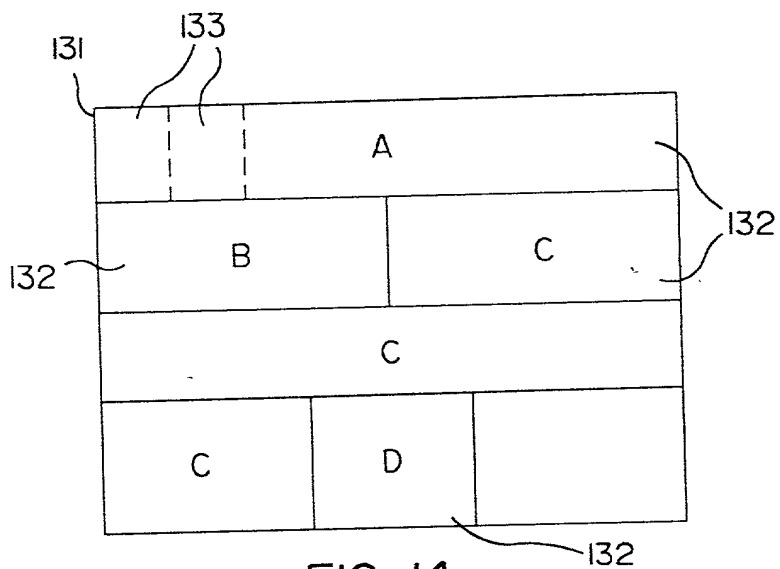


FIG. 13



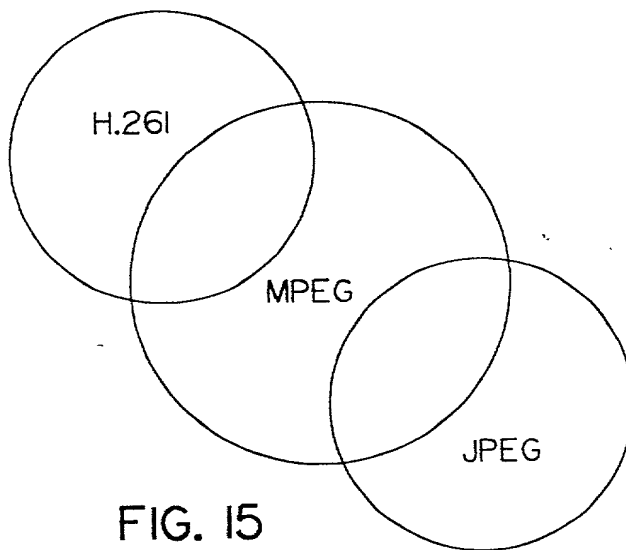


FIG. 15

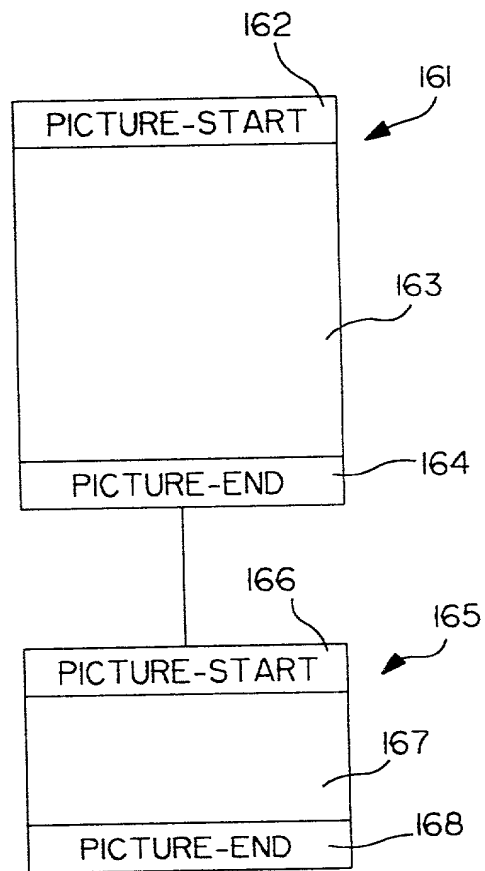
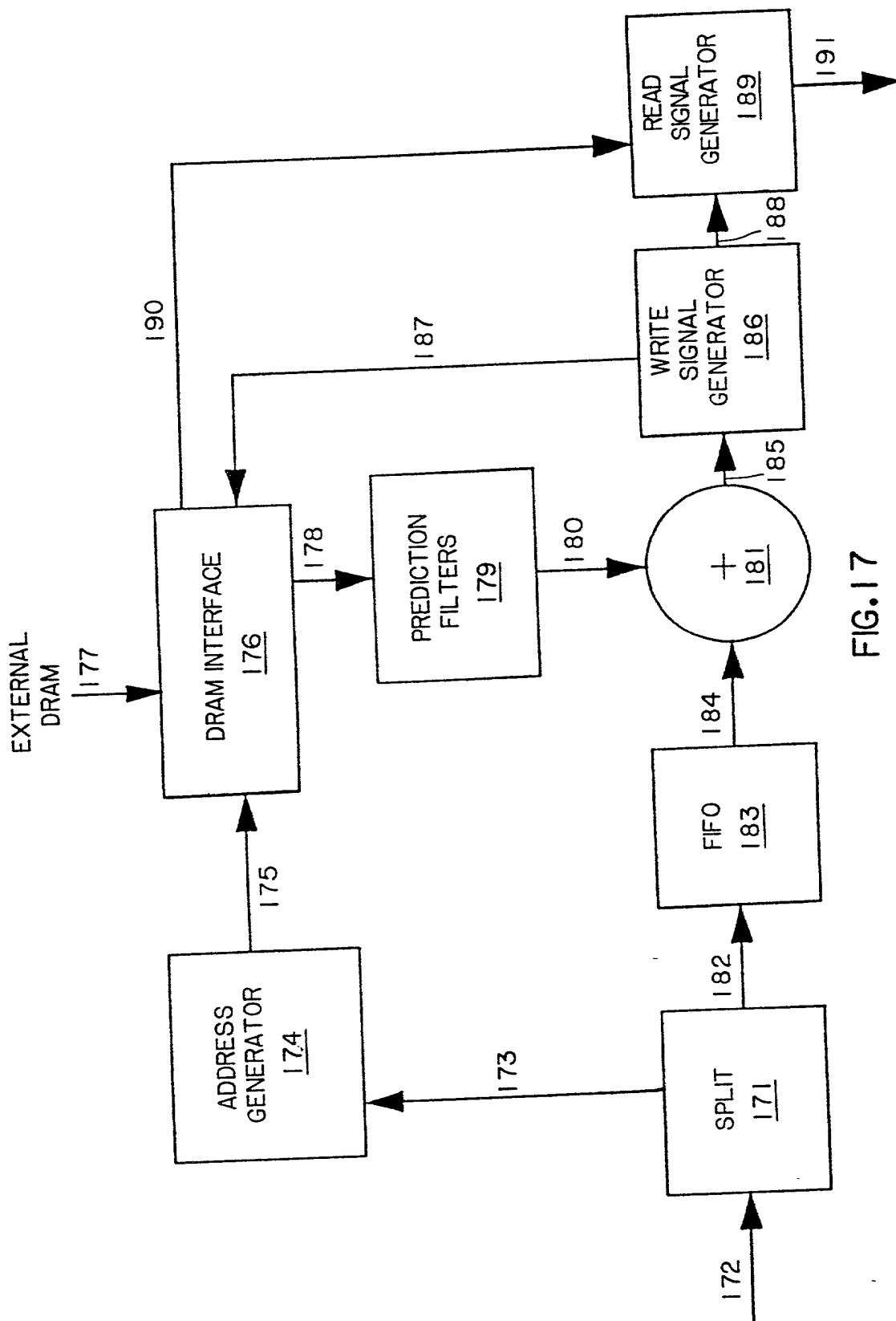


FIG. 16



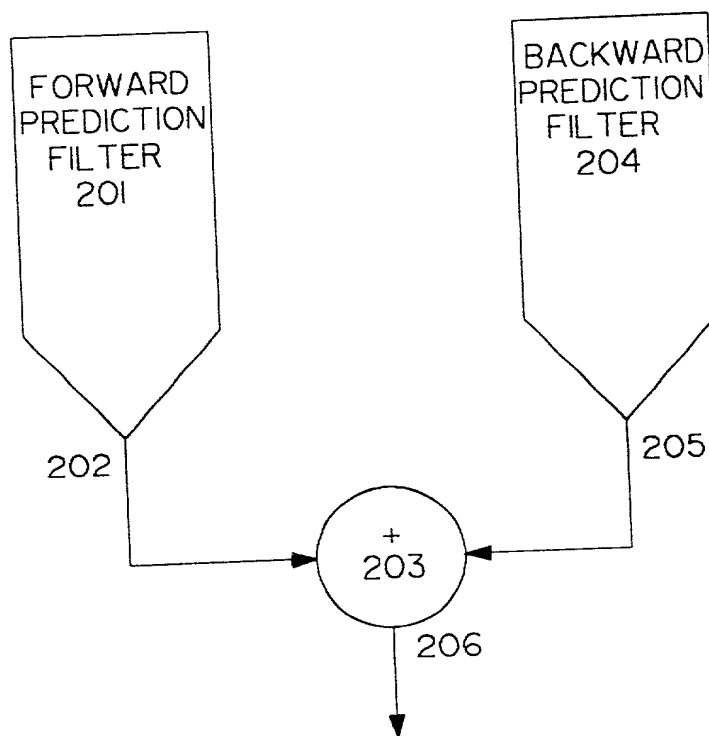


FIG. 18

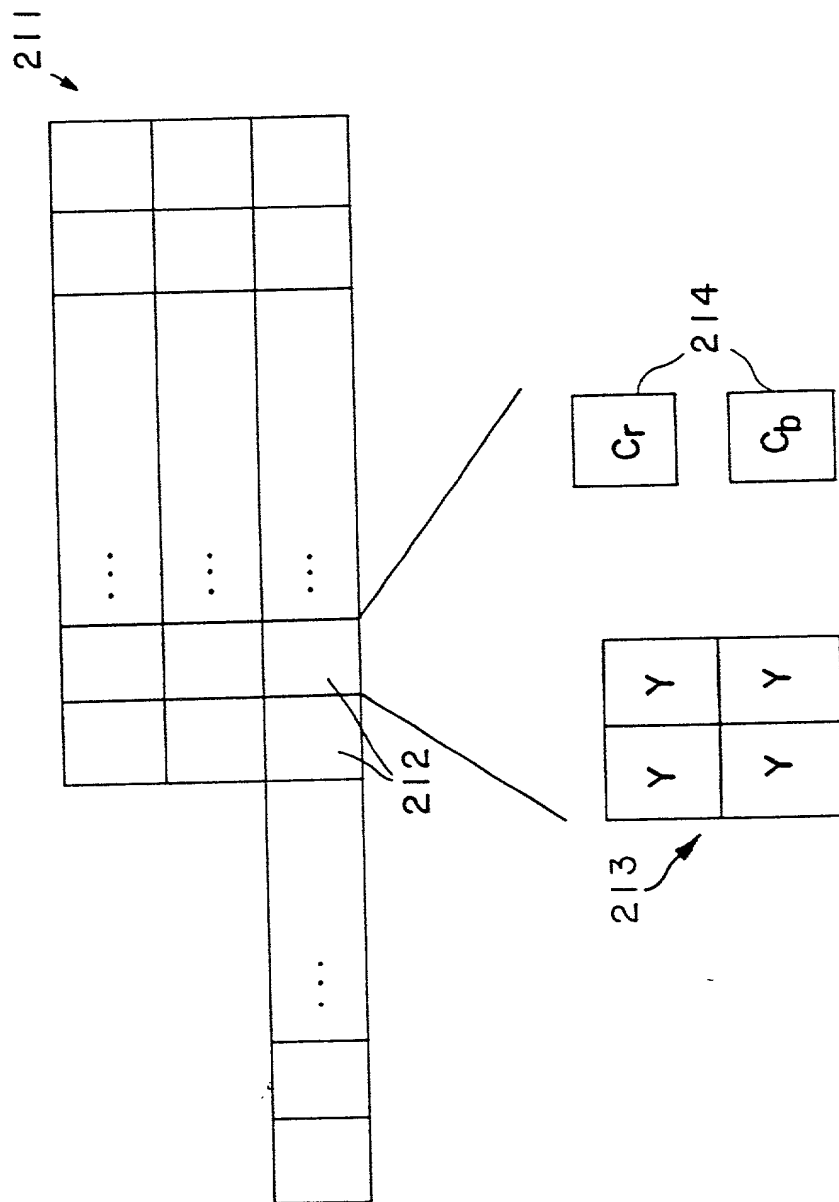


FIG. 19

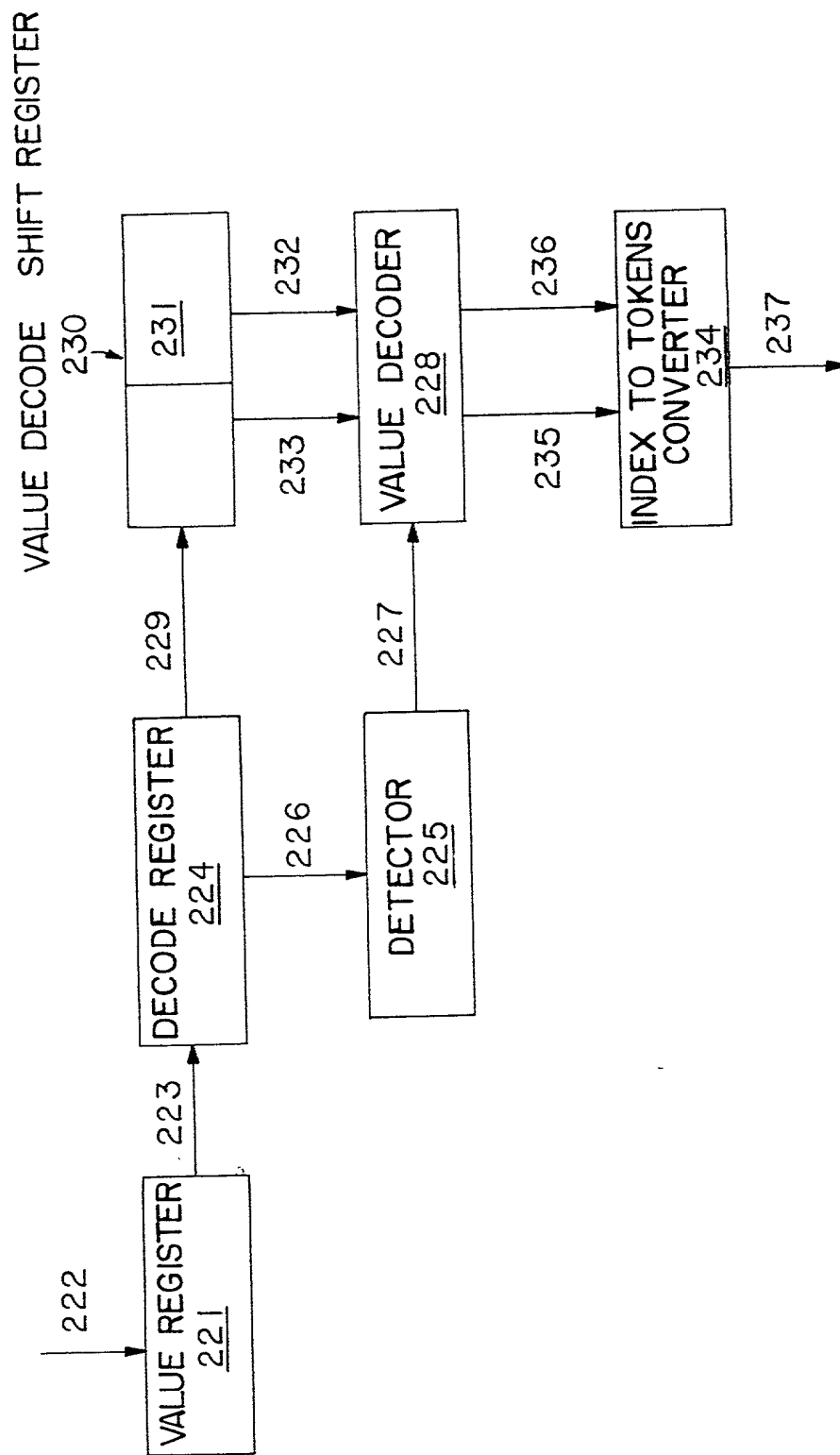


FIG.20

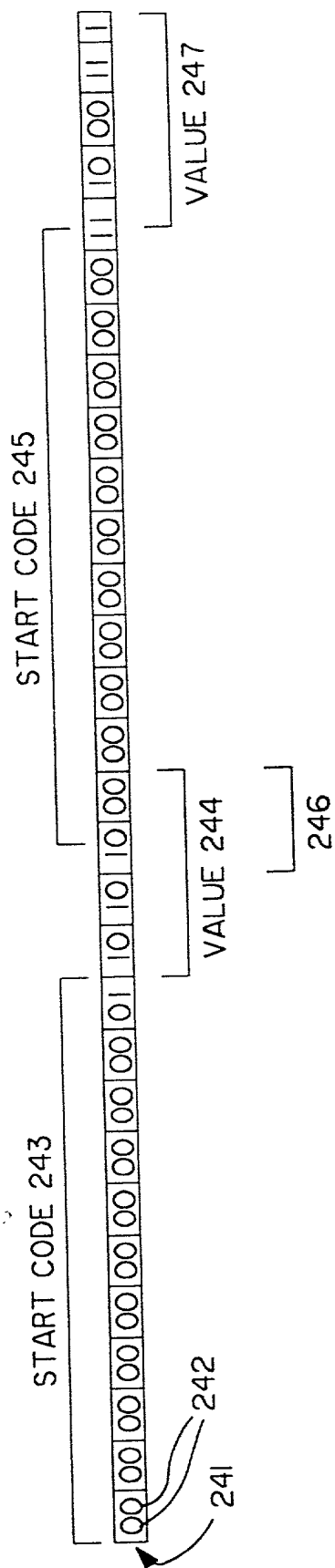


FIG. 21

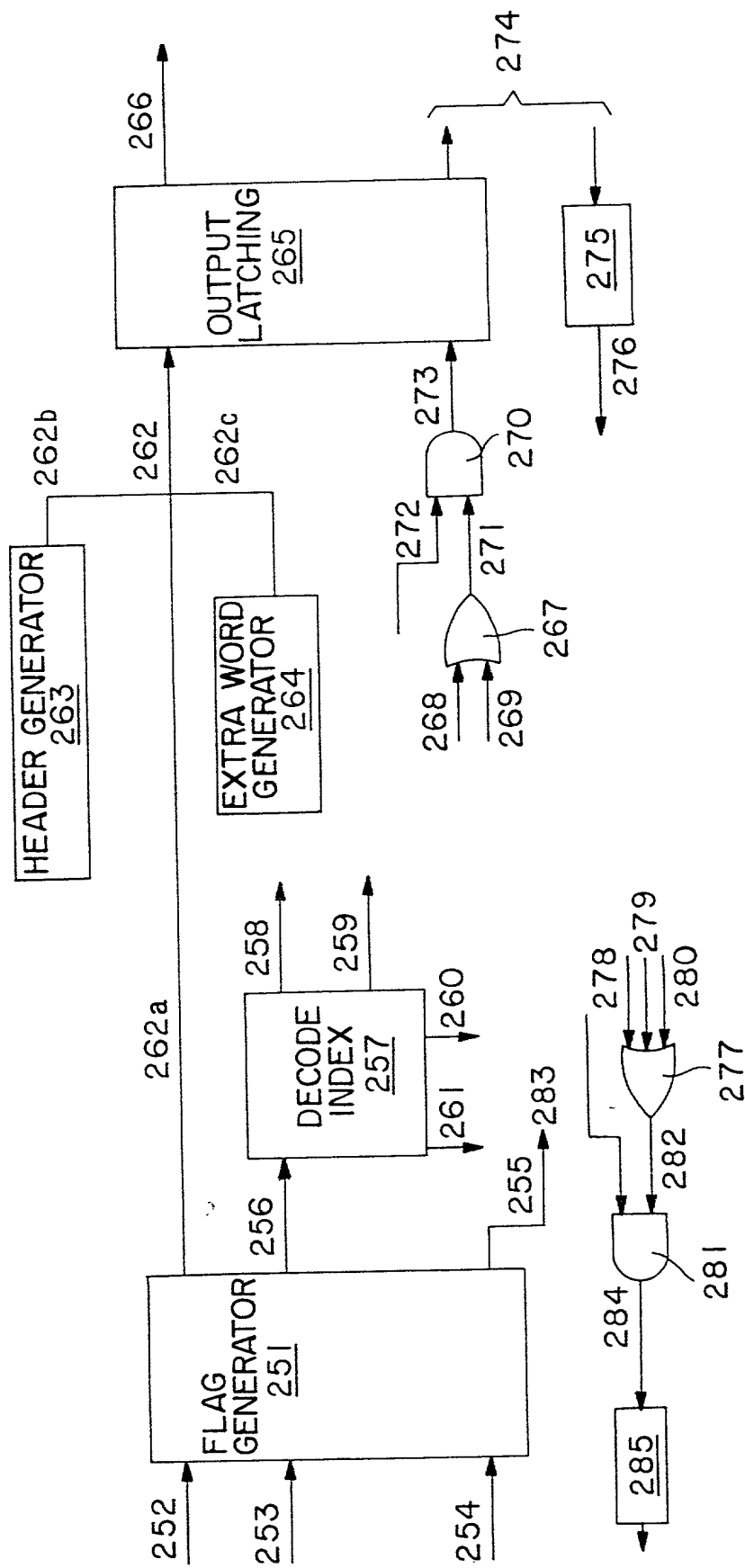


FIG. 22

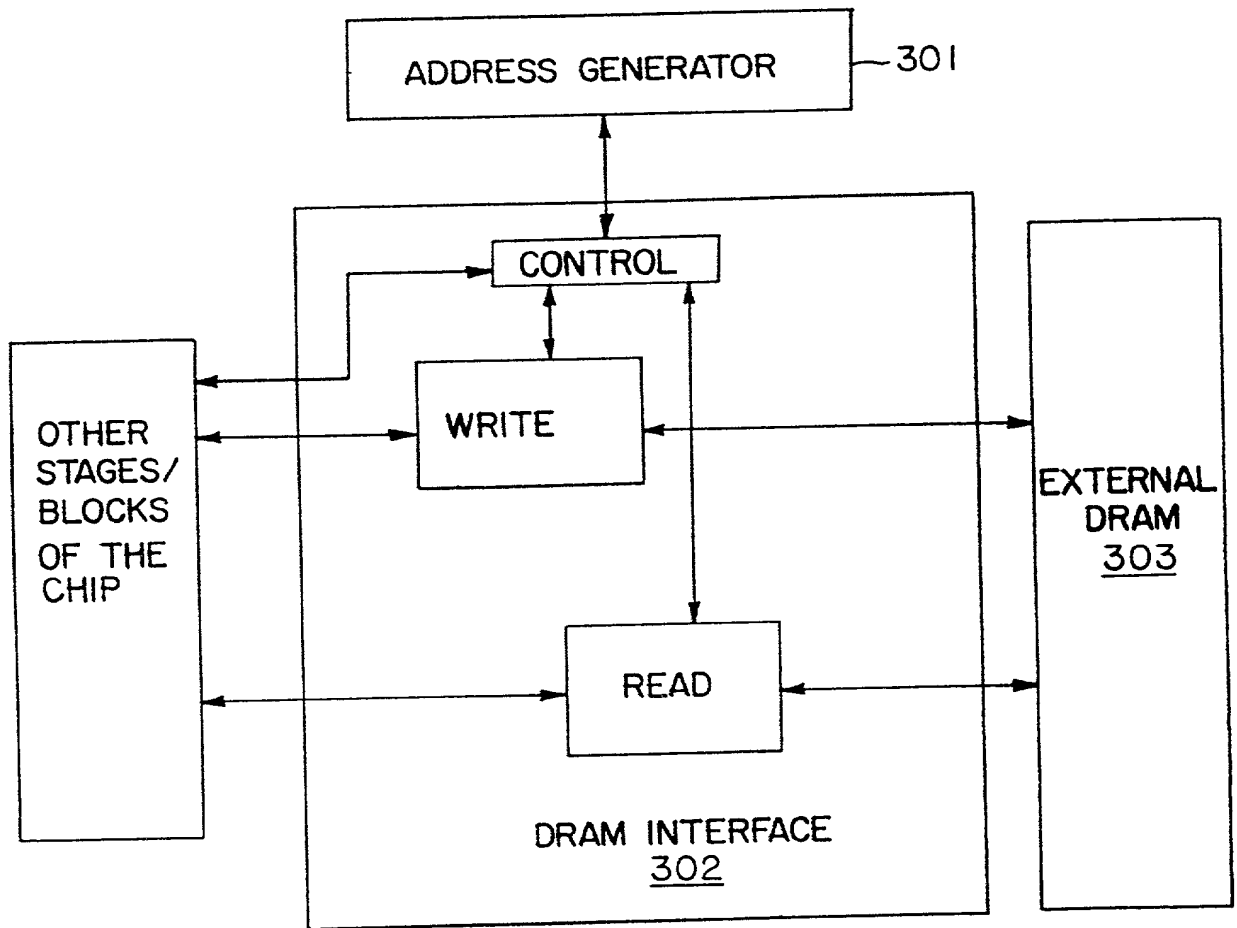


FIG.23

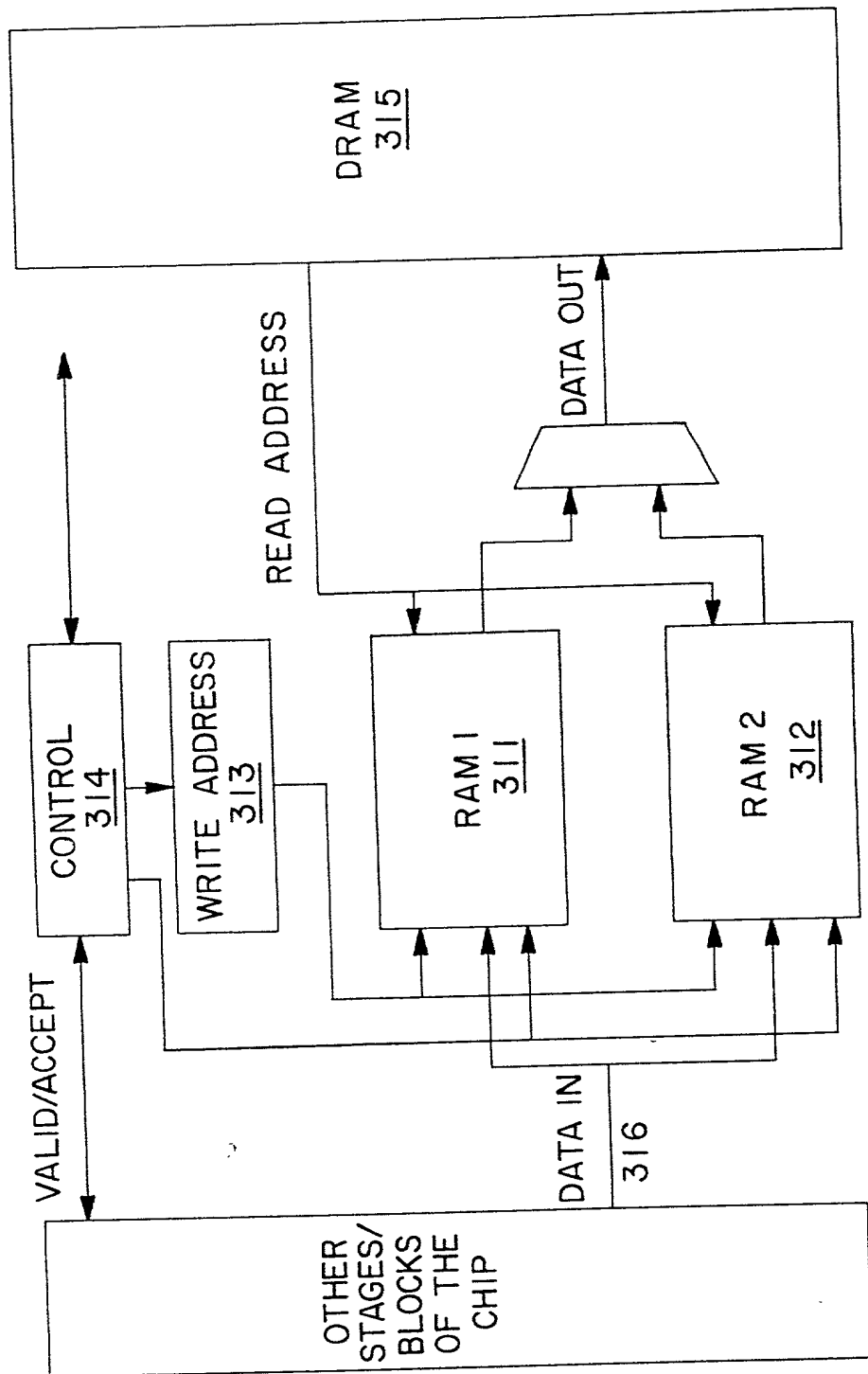


FIG.24

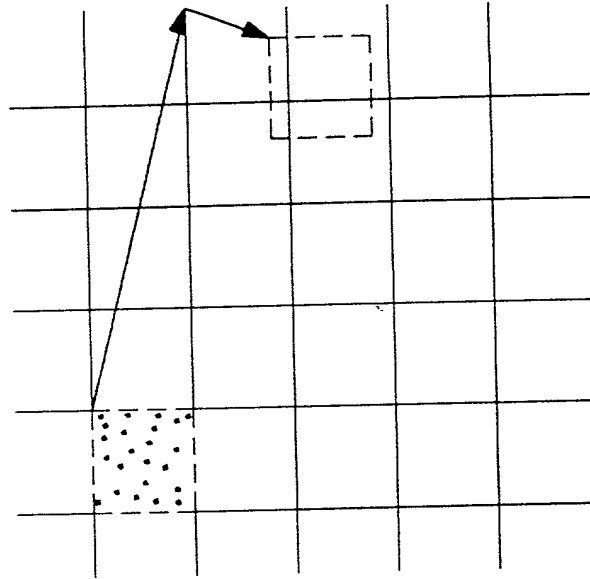


FIG. 25

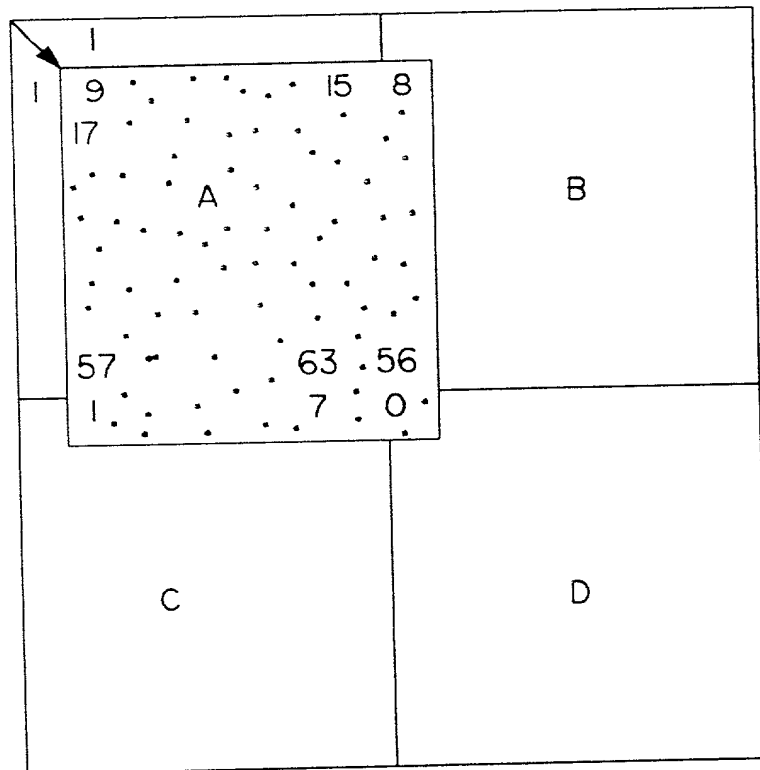


FIG. 26

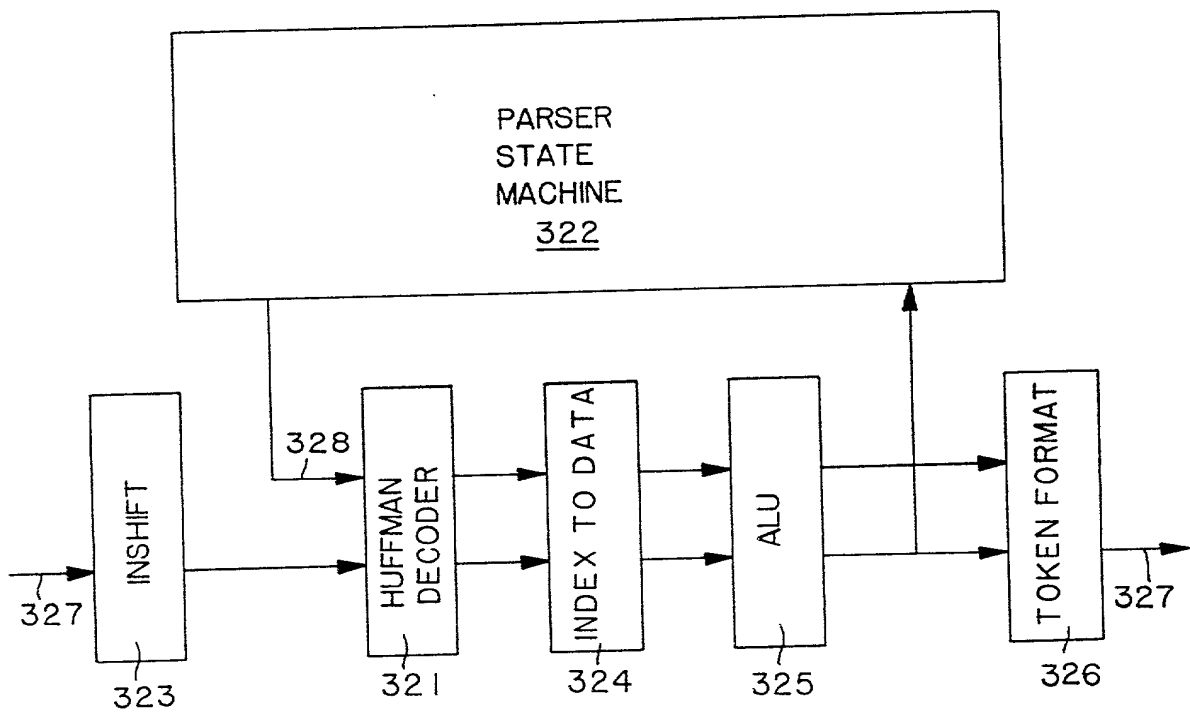


FIG.27

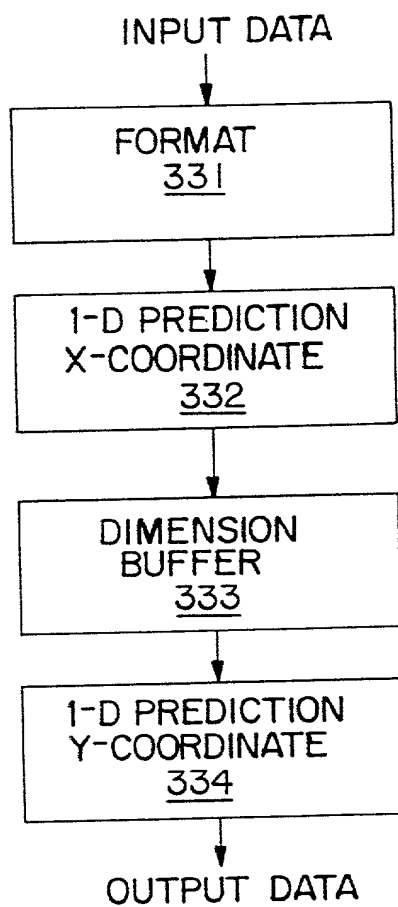


FIG.28

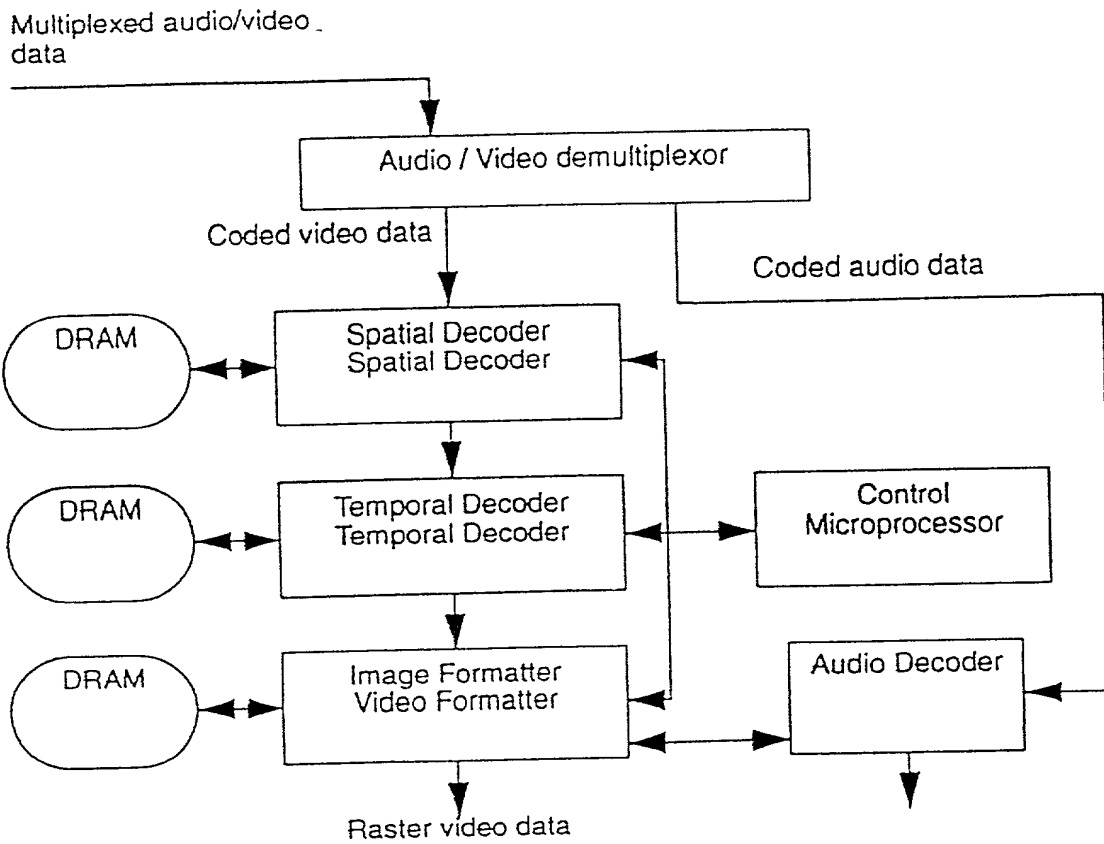


FIG.29

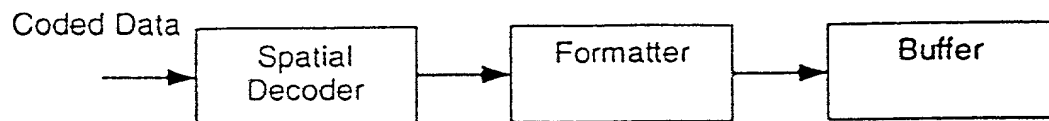


FIG.30

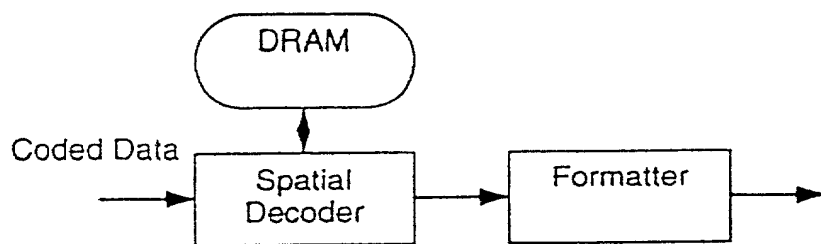


FIG.31

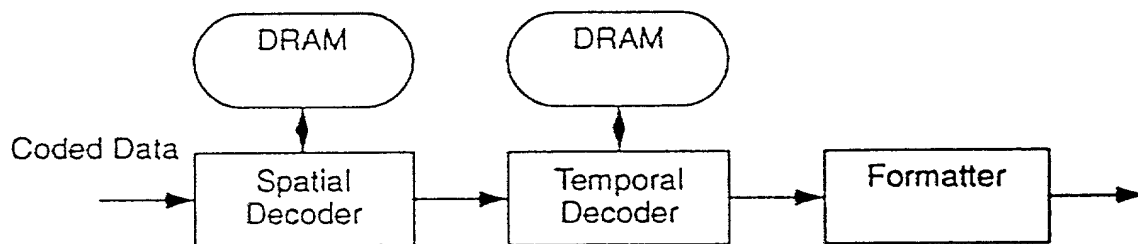


FIG.32

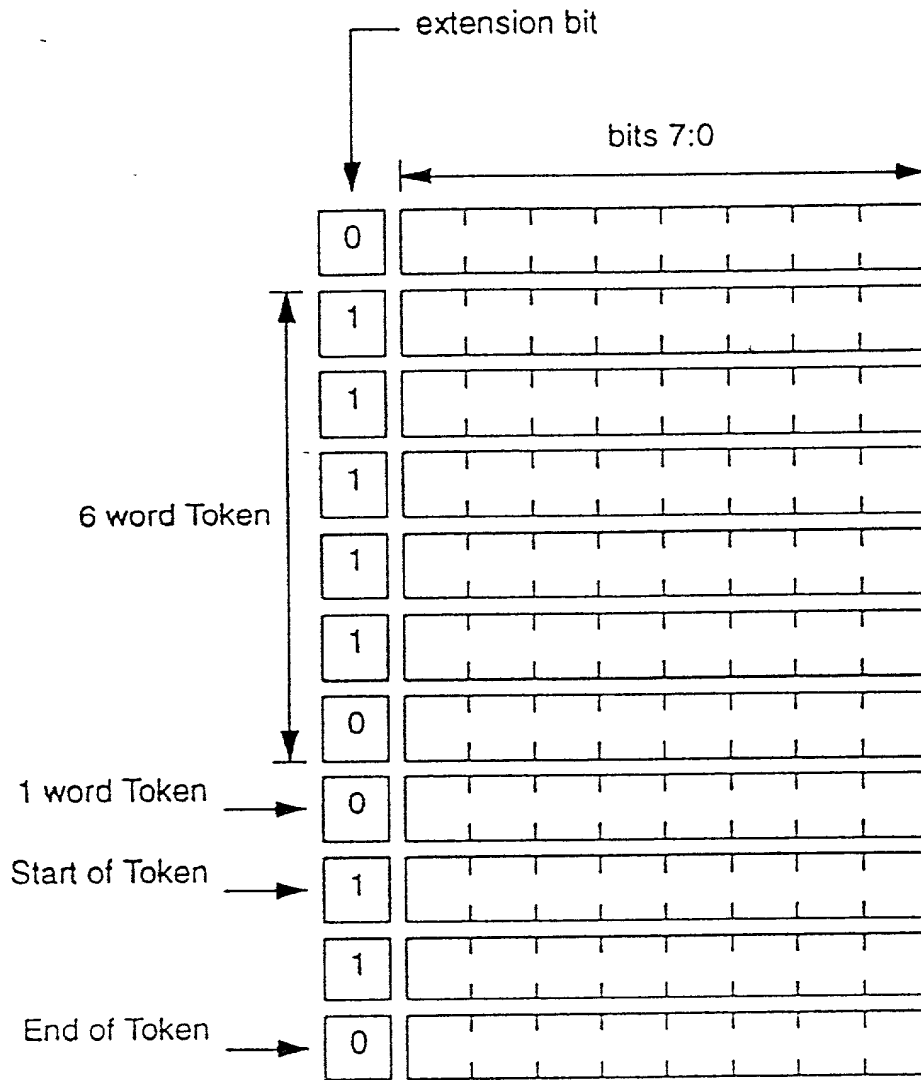


FIG.33

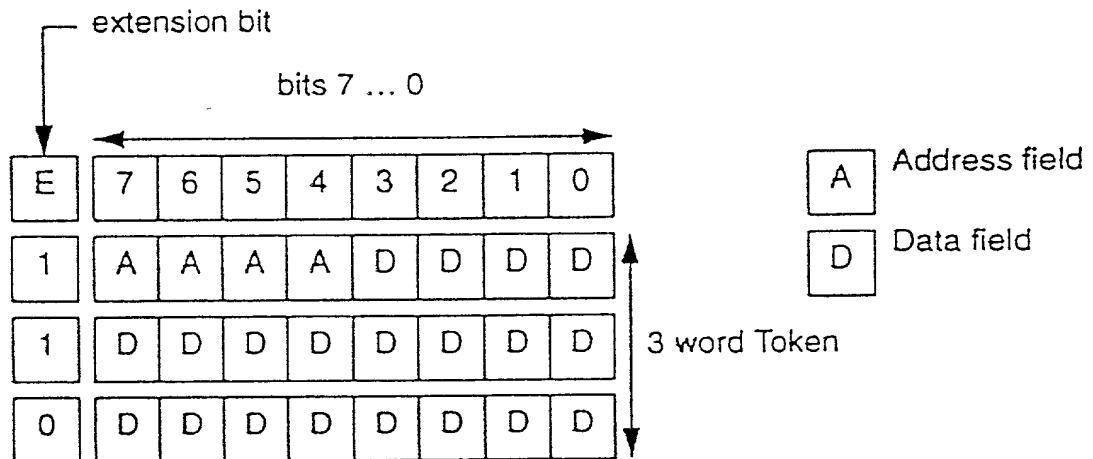


FIG.34

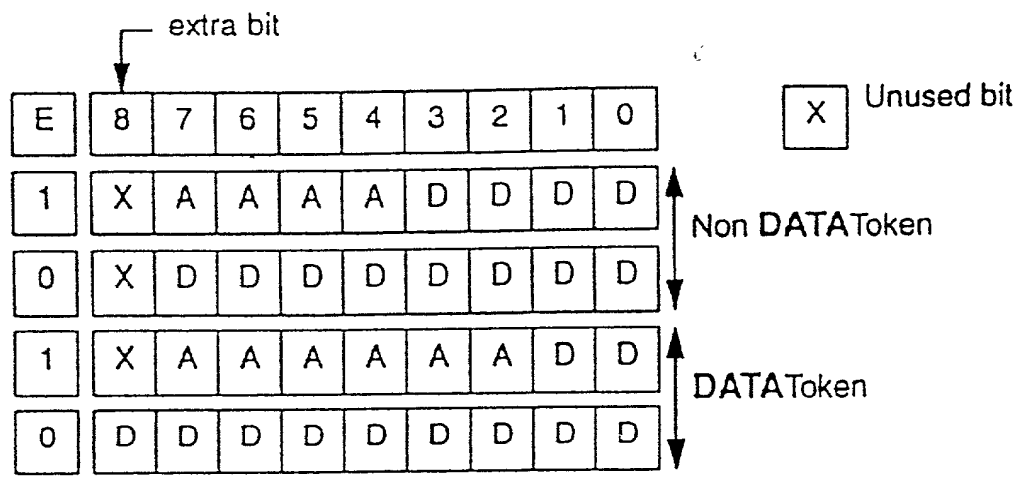
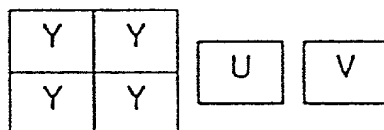


FIG.35



MPEG 4:2:0
macroblock

FIG.36A



JPEG 2:1:1
macroblock

FIG.36B

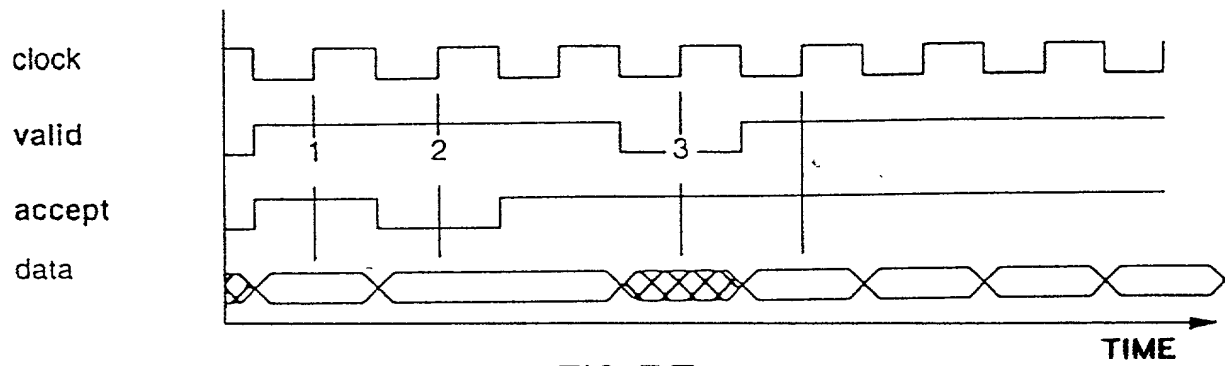


FIG.37

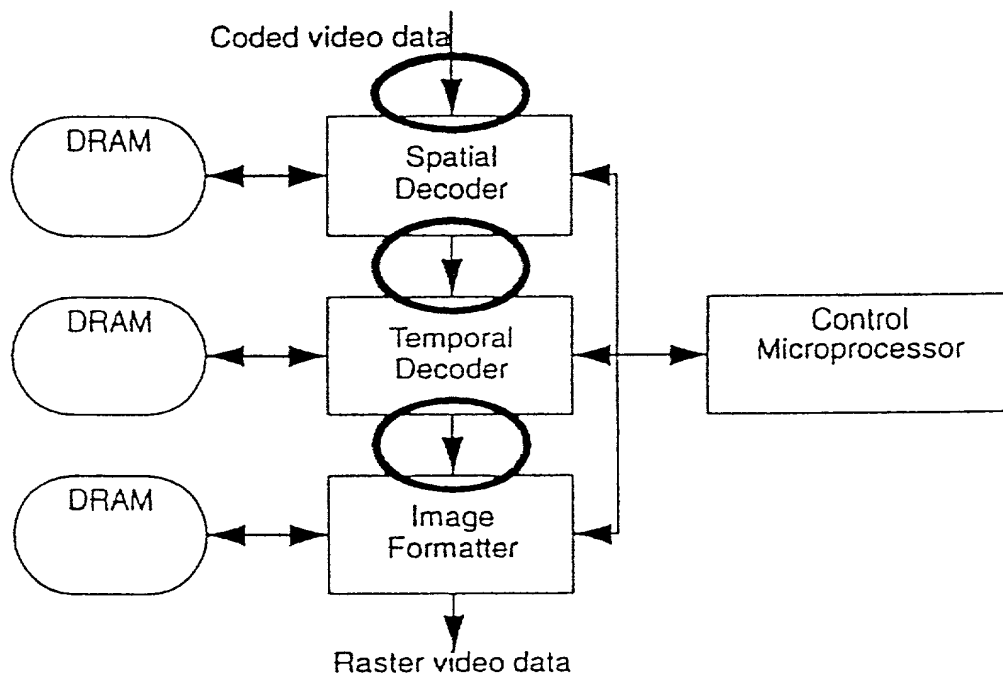


FIG.38

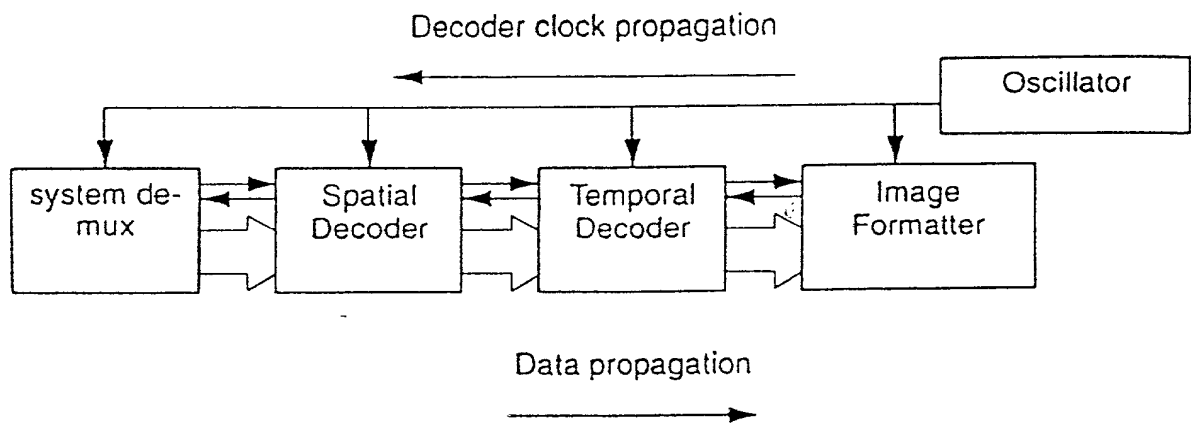


FIG.39

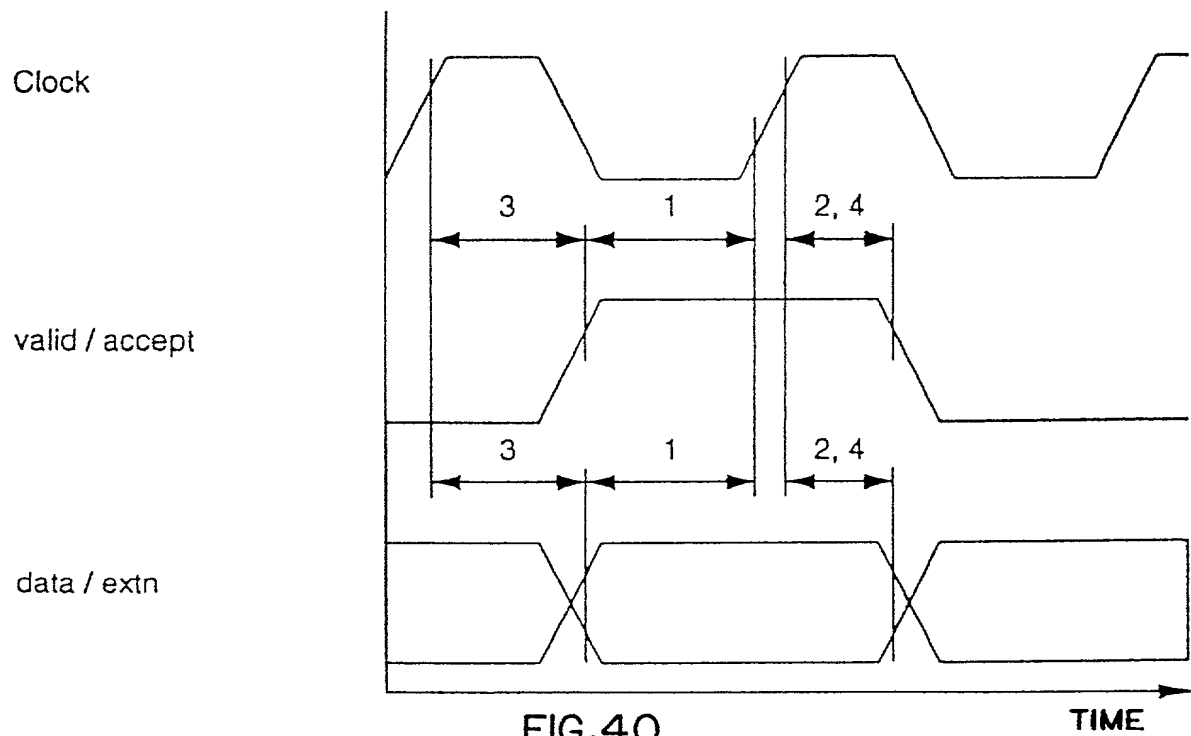


FIG.40

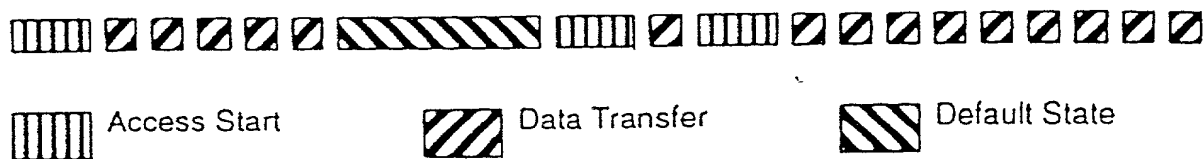


FIG.41

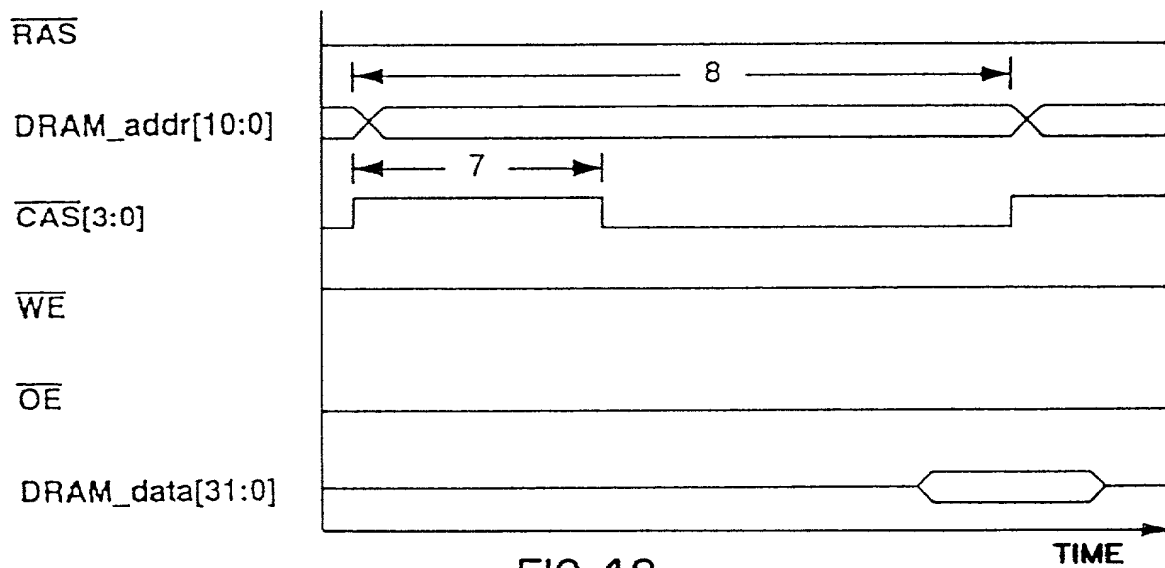


FIG.42

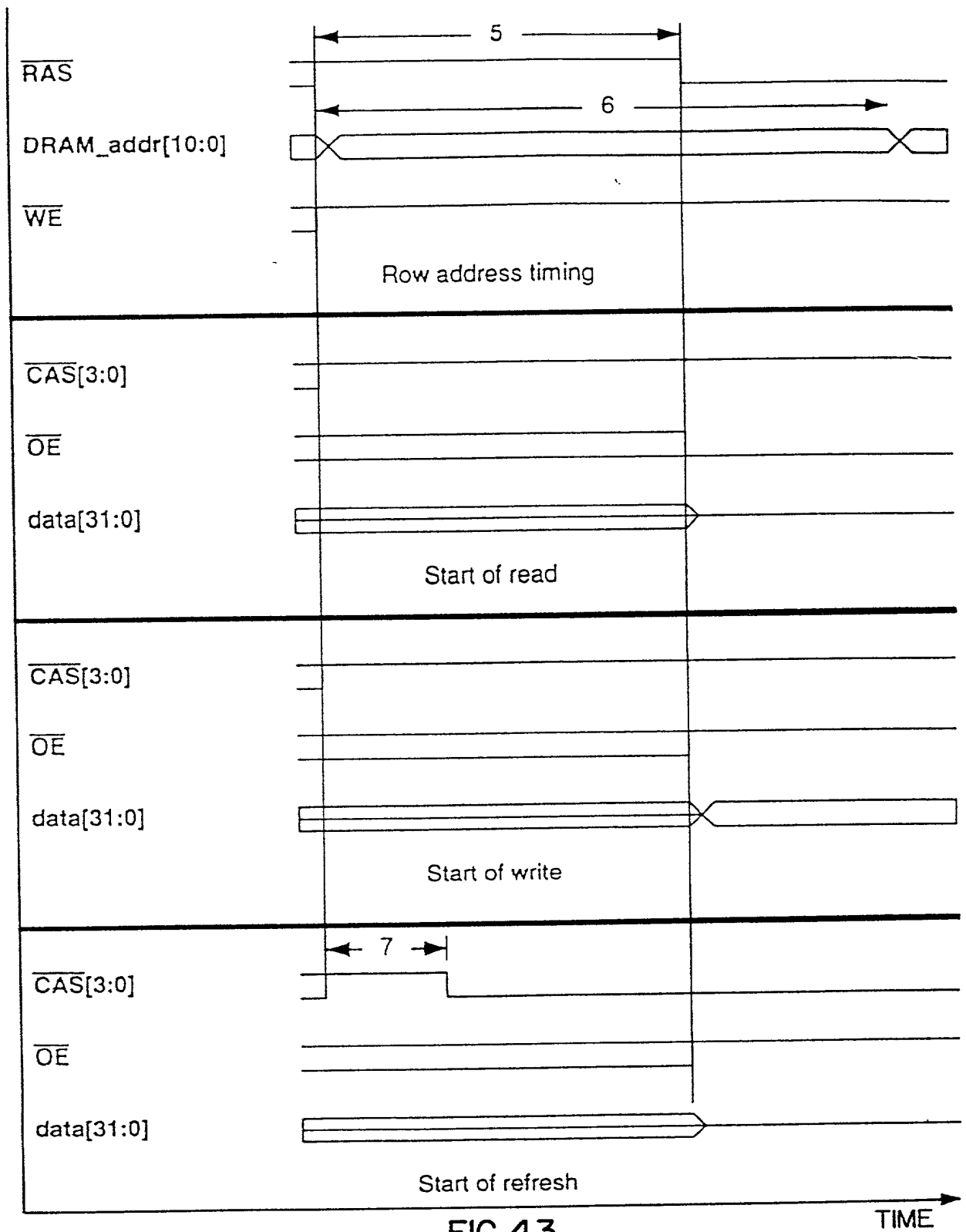


FIG.43

$\overline{\text{RAS}}$

DRAM_addr[10:0]

$\overline{\text{CAS}}[3:0]$

$\overline{\text{WE}}$

$\overline{\text{OE}}$

DRAM_data[31:0]

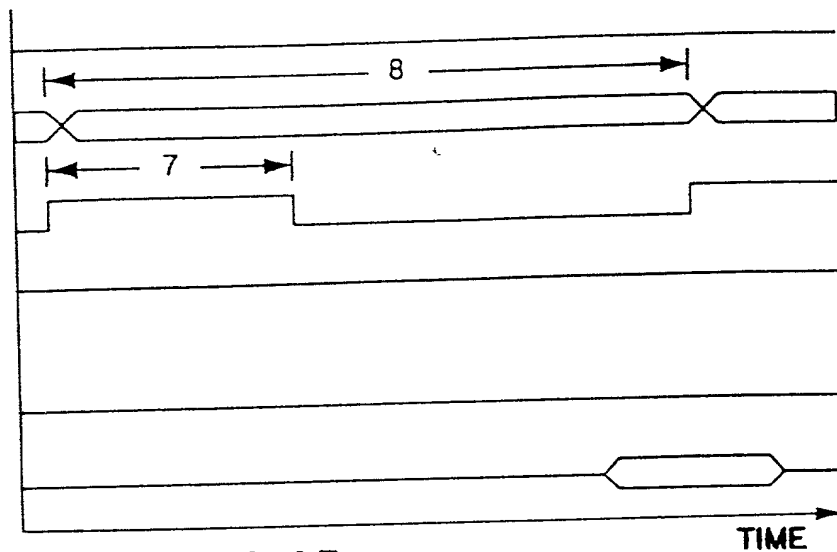


FIG.45

$\overline{\text{RAS}}$

DRAM_addr[10:0]

$\overline{\text{CAS}}[3:0]$

$\overline{\text{WE}}$

$\overline{\text{OE}}$

DRAM_data[31:0]

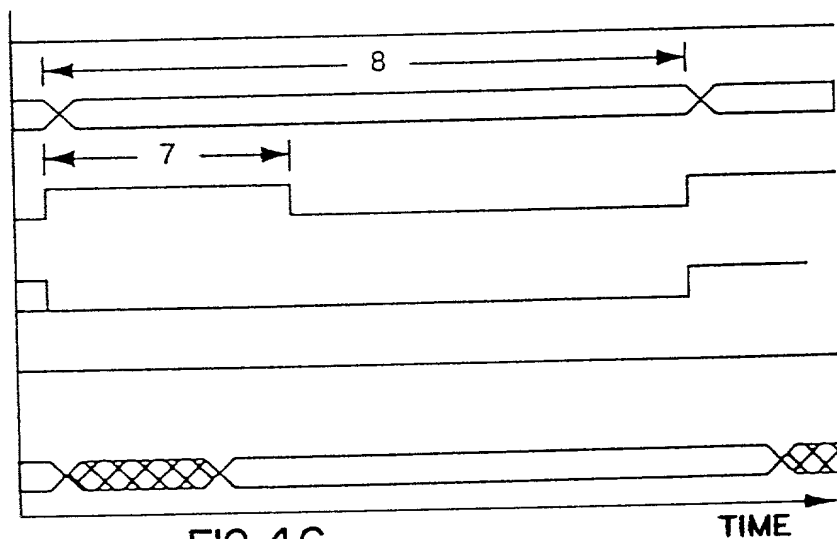


FIG.46

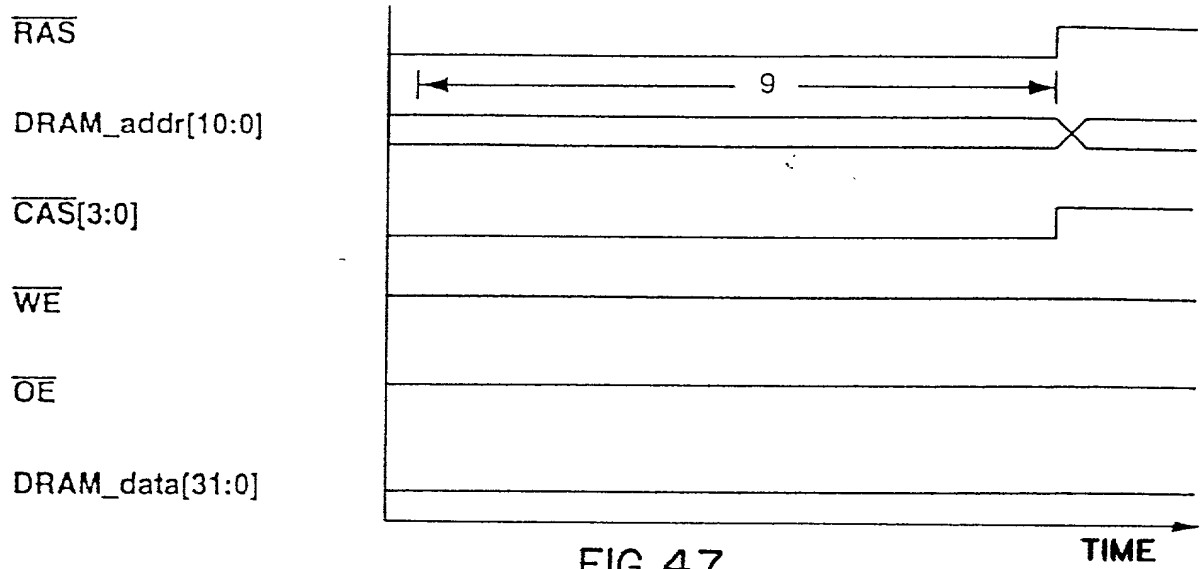


FIG.47

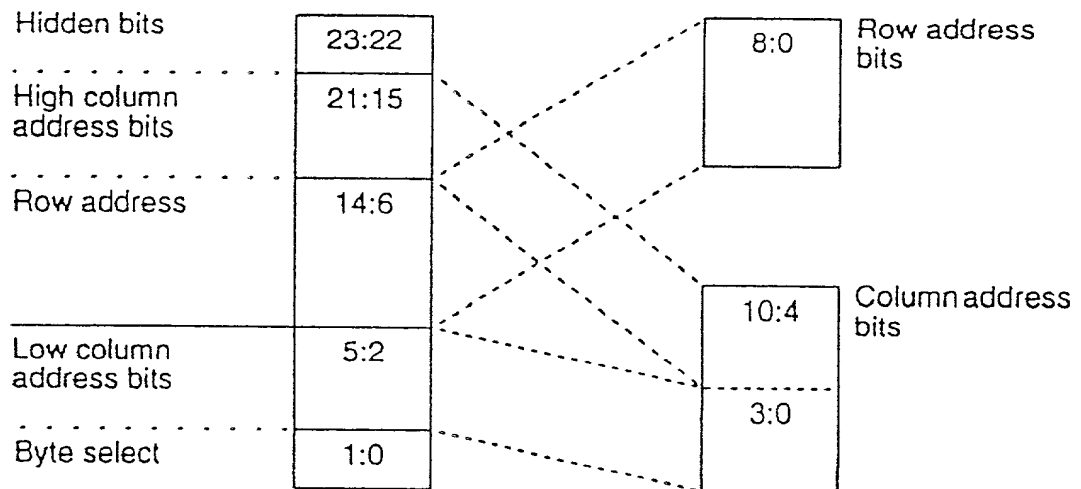


FIG.48

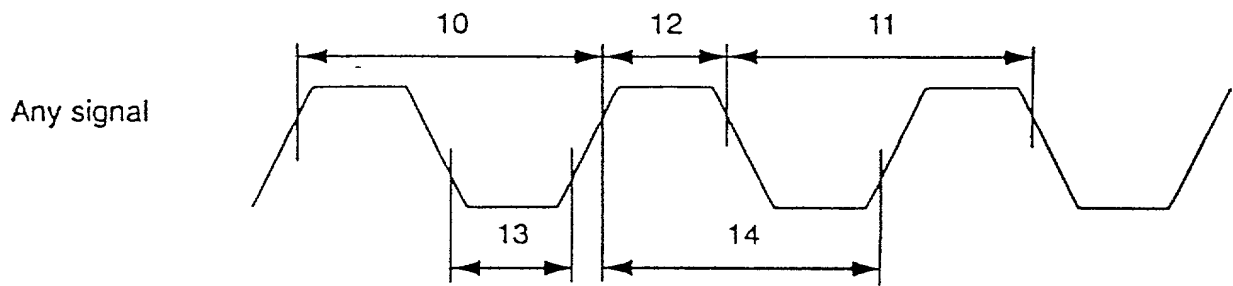


FIG. 49

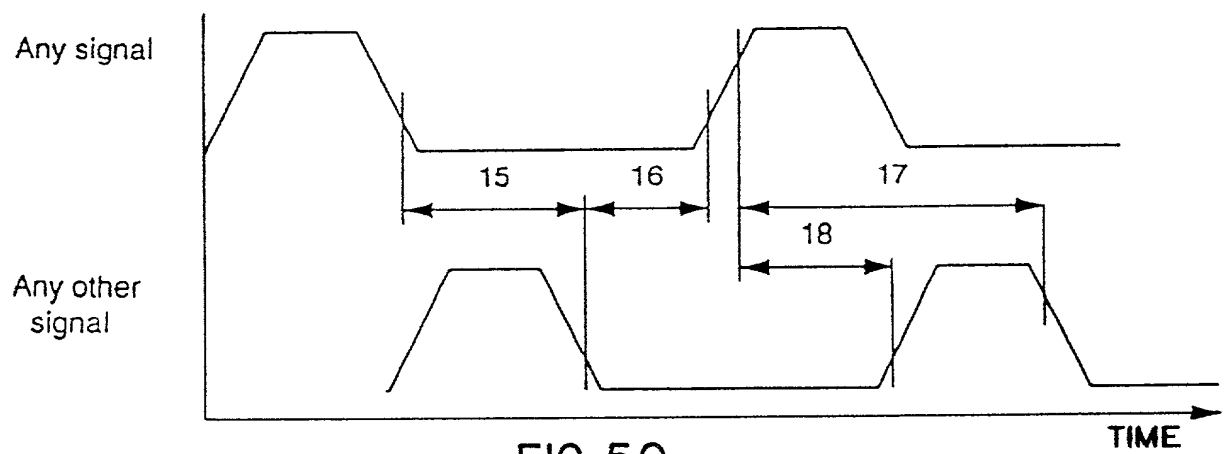


FIG. 50

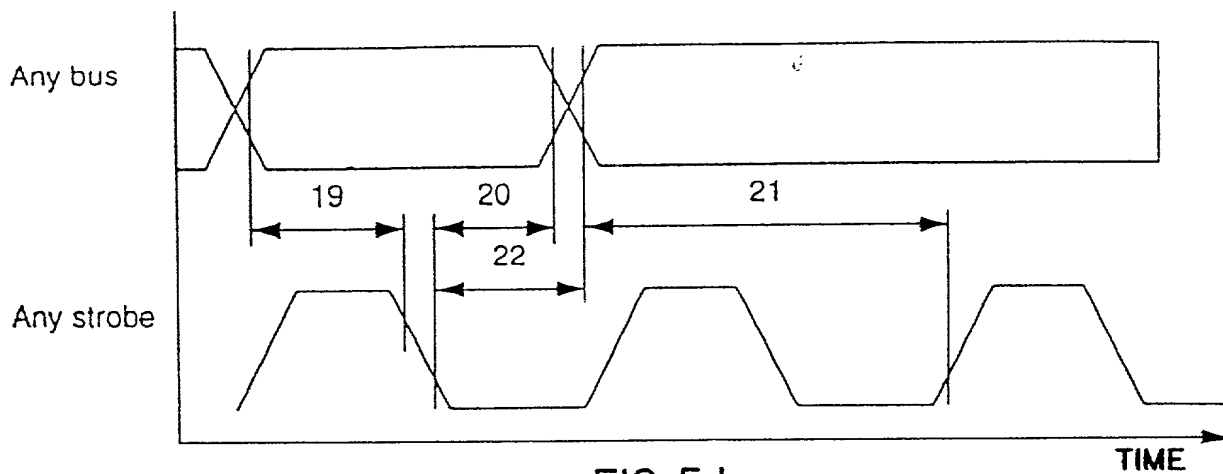


FIG.51

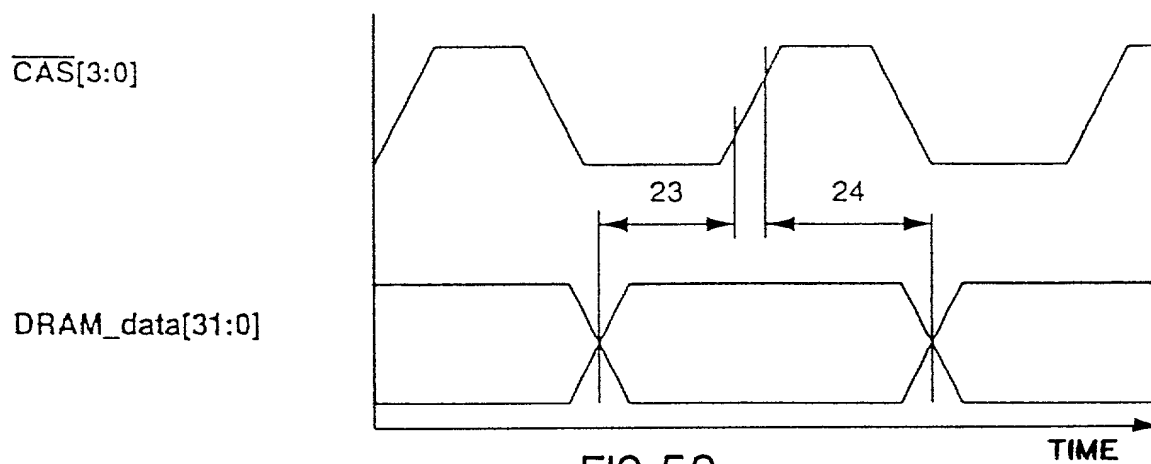


FIG.52

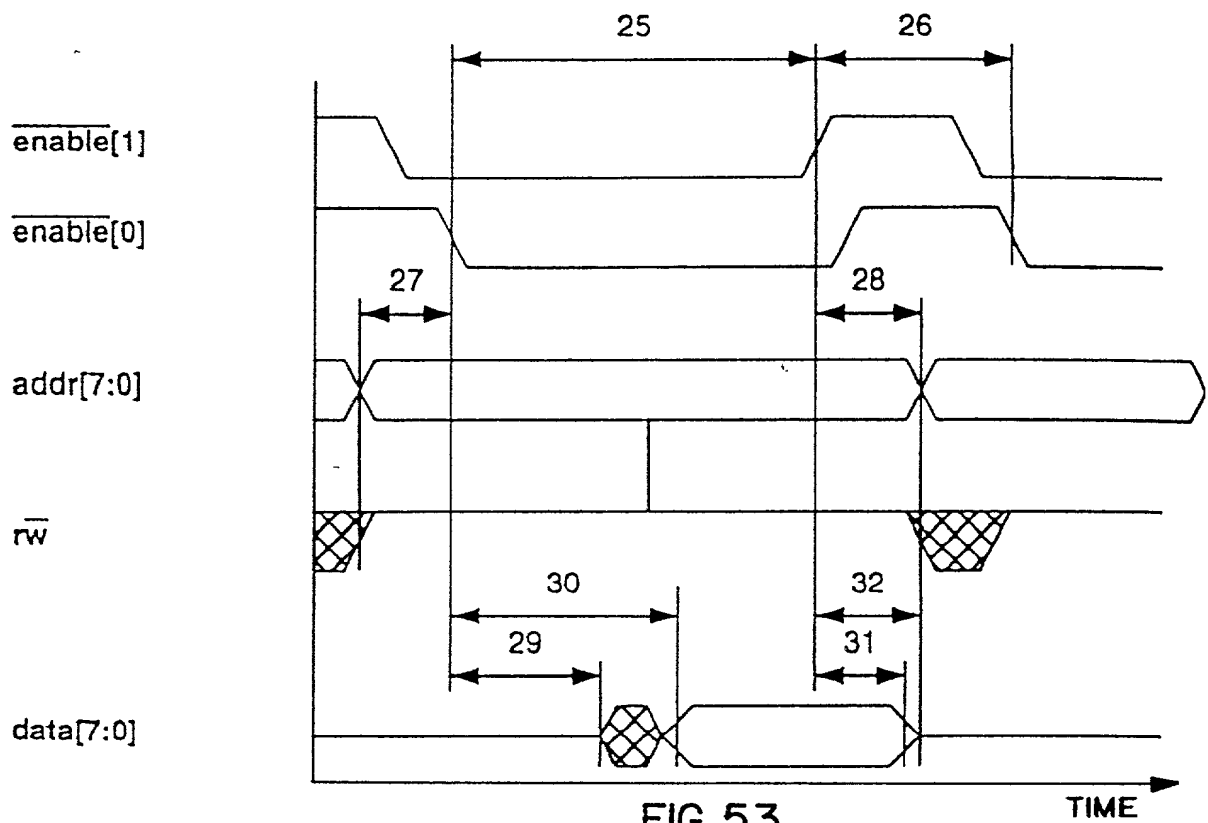


FIG.53

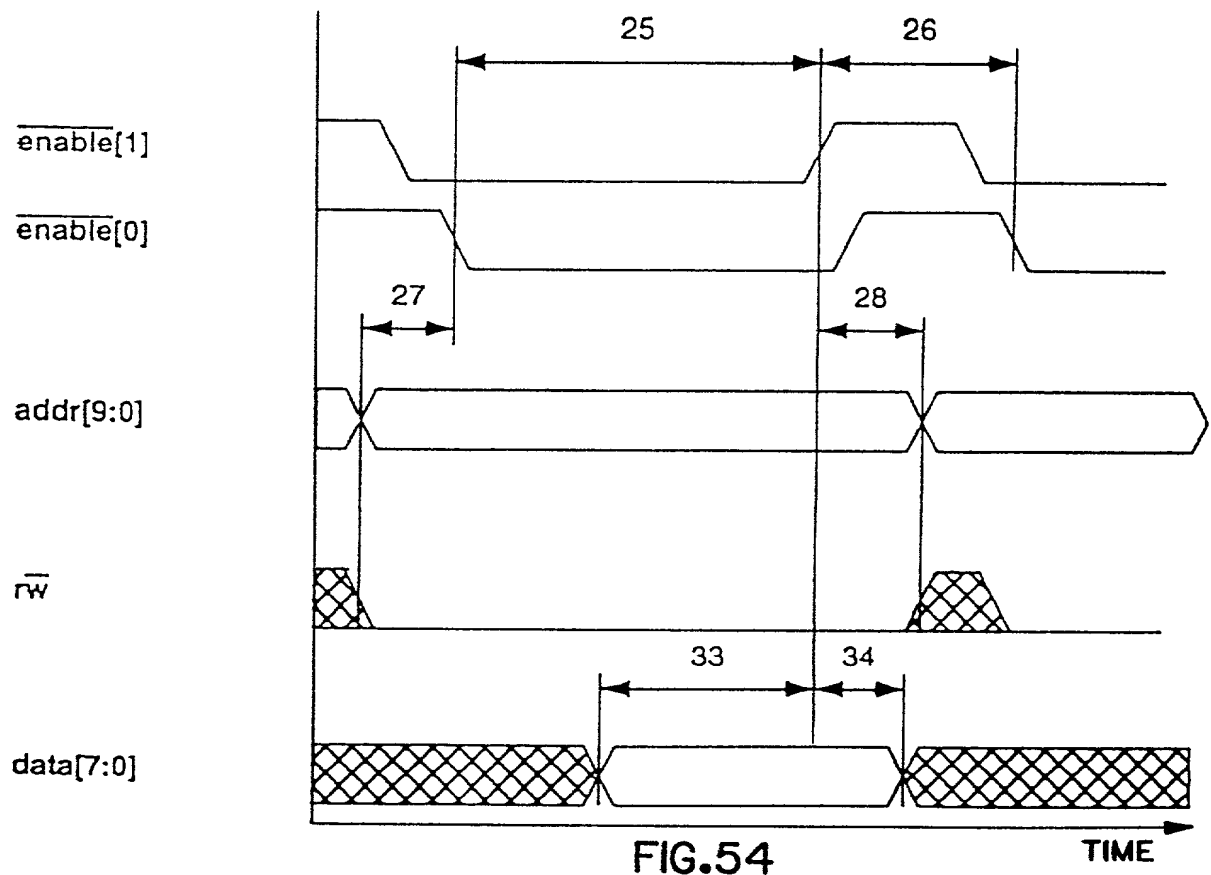


FIG.54

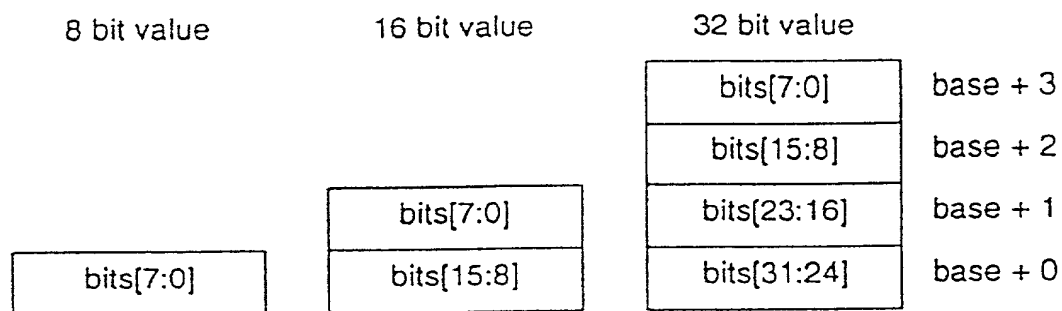


FIG.55

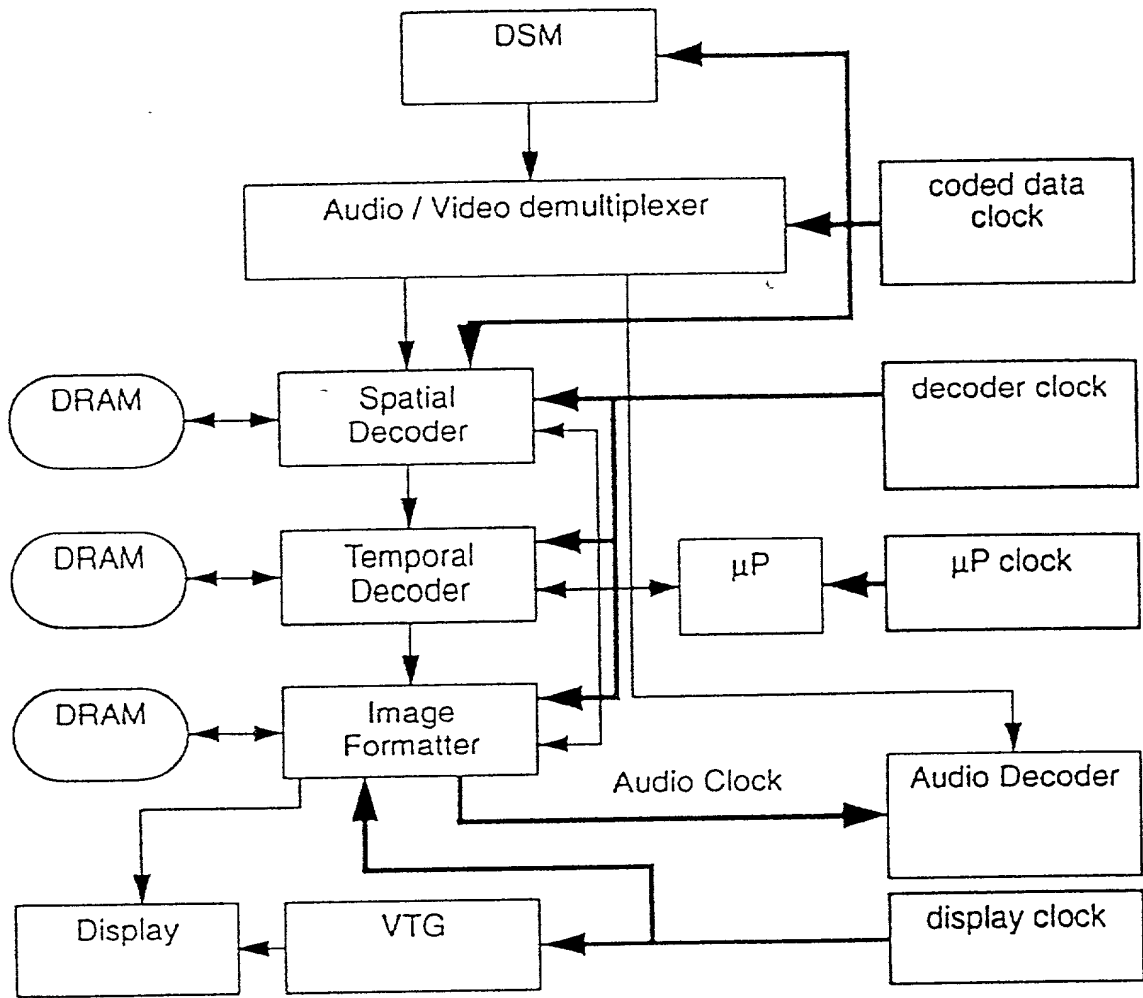


FIG.56

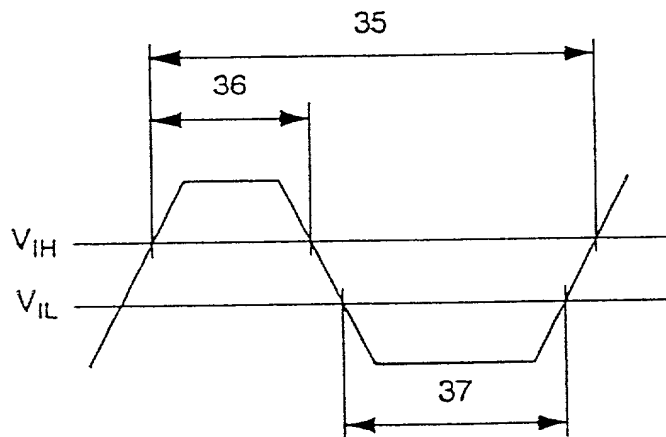


FIG.57

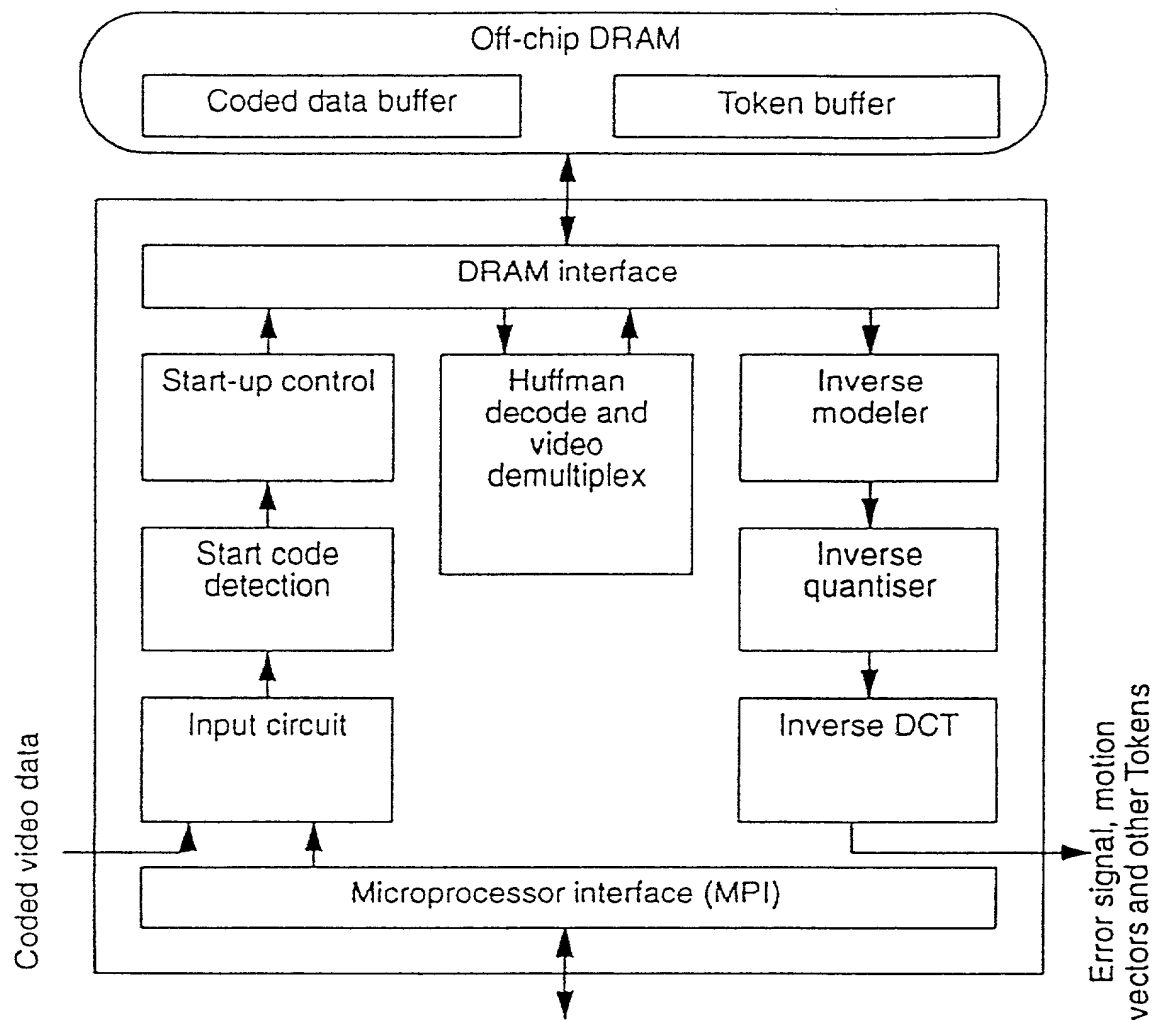


FIG.58

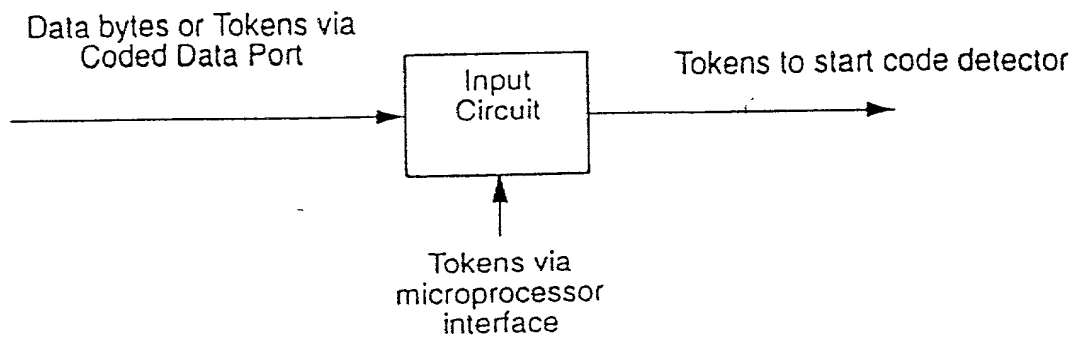


FIG.59

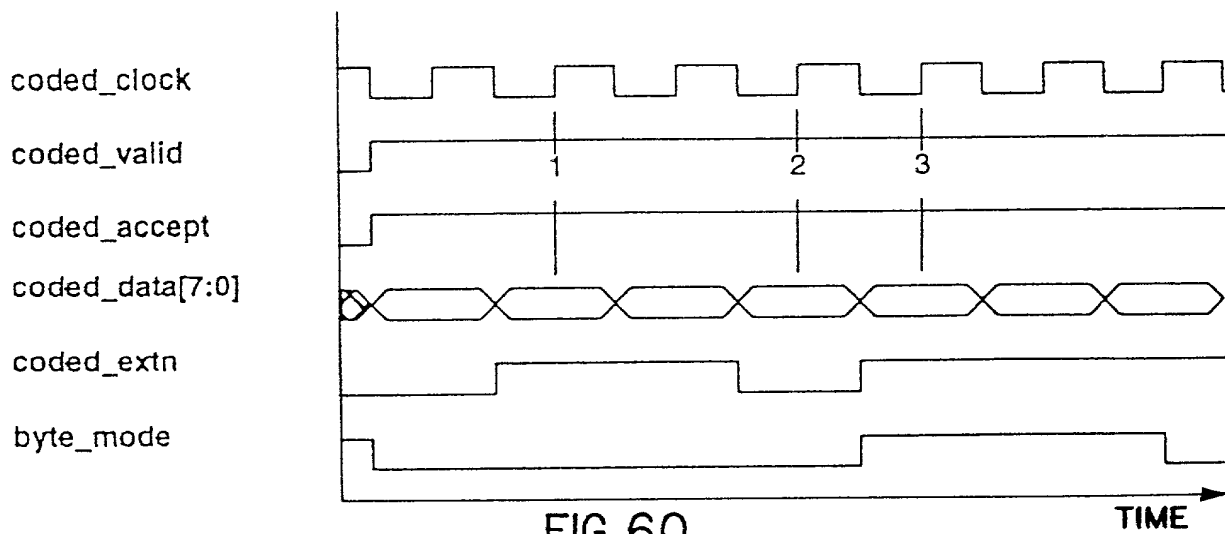


FIG.60

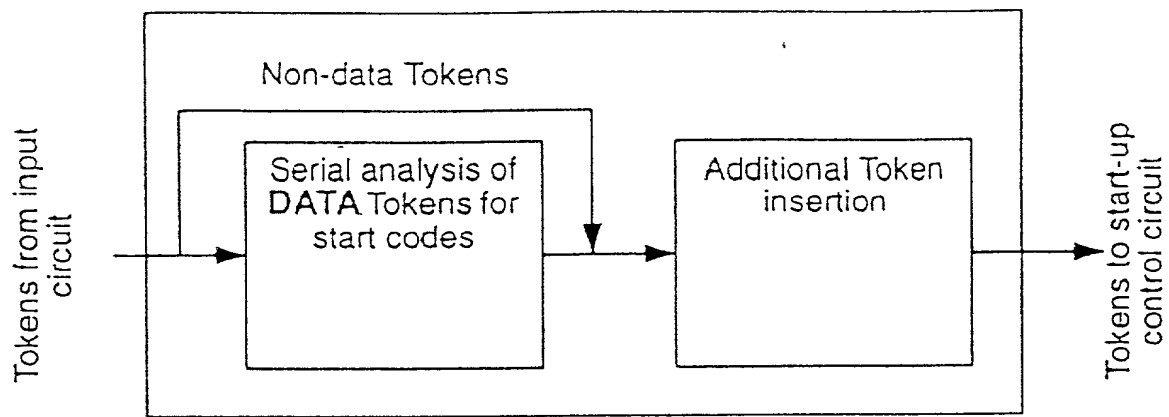


FIG.61

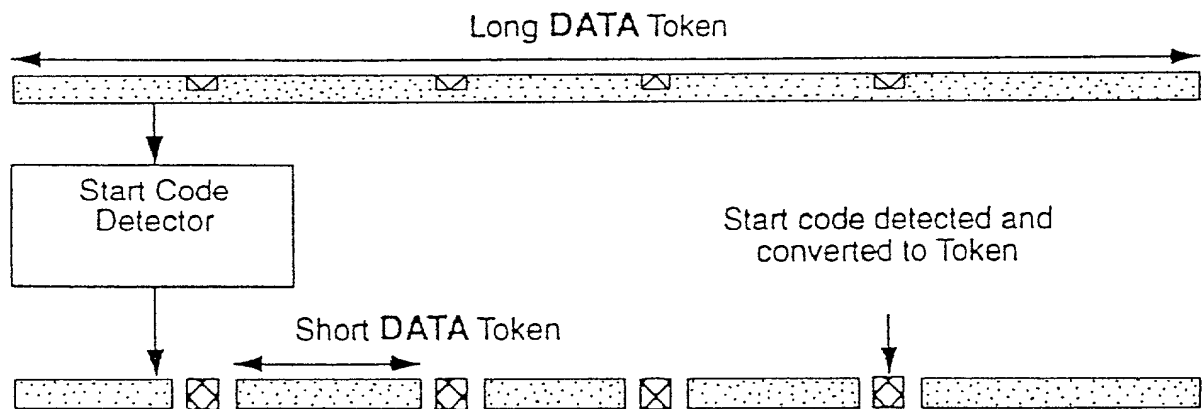


FIG.62

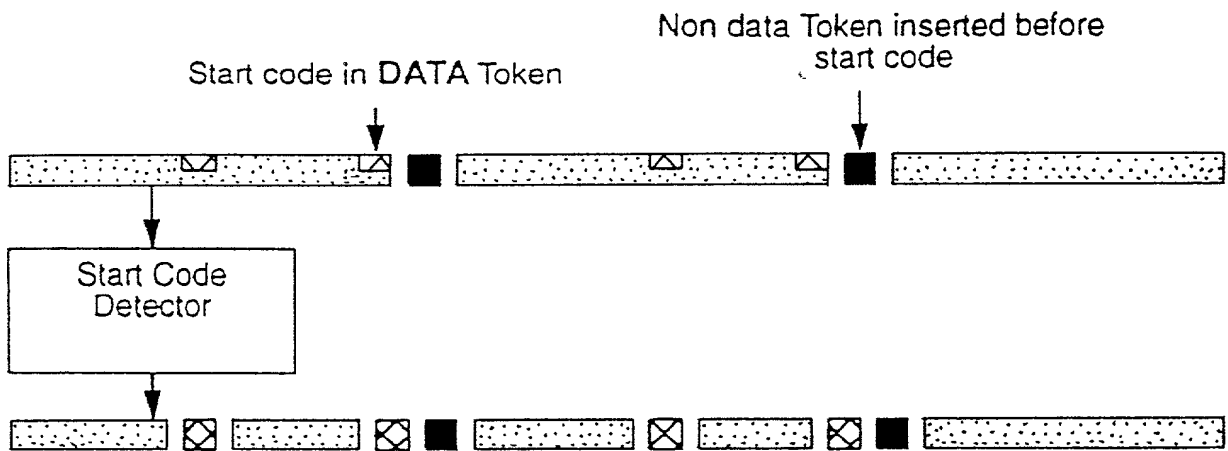


FIG.63

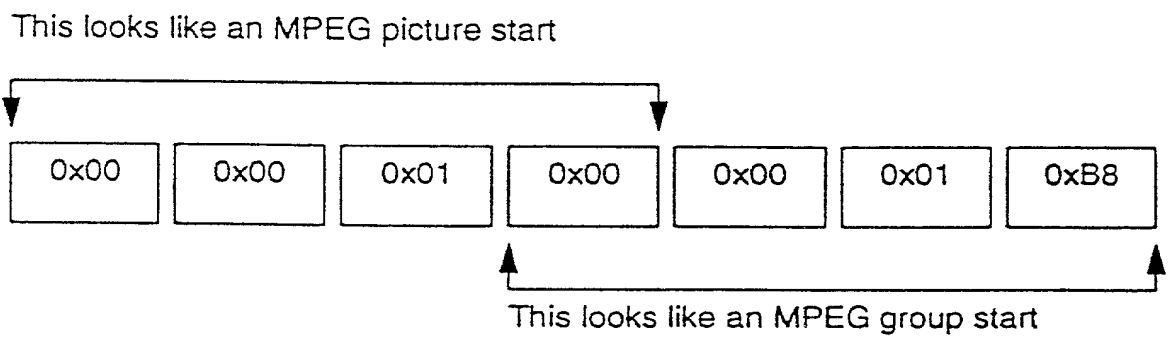


FIG.64

This looks like an MPEG slice start (0x28)

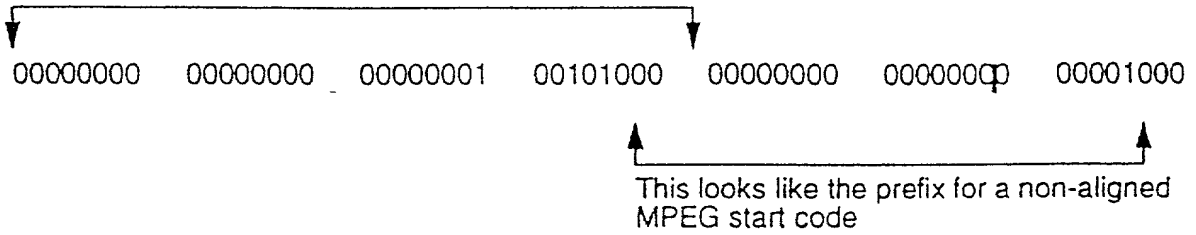


FIG.65

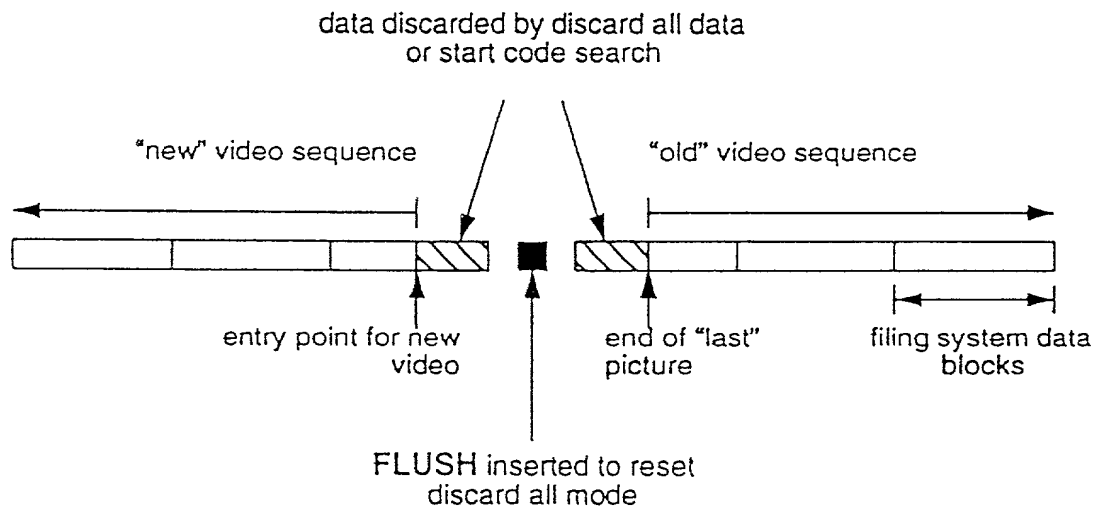


FIG.66

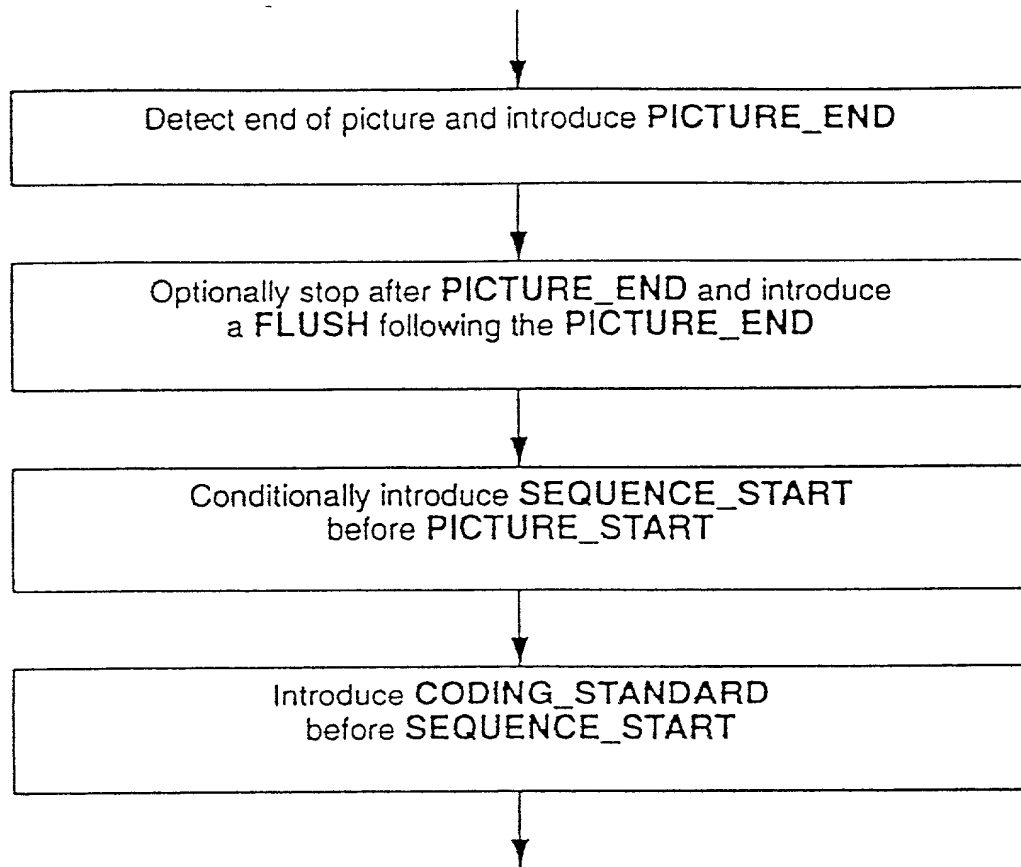


FIG.67

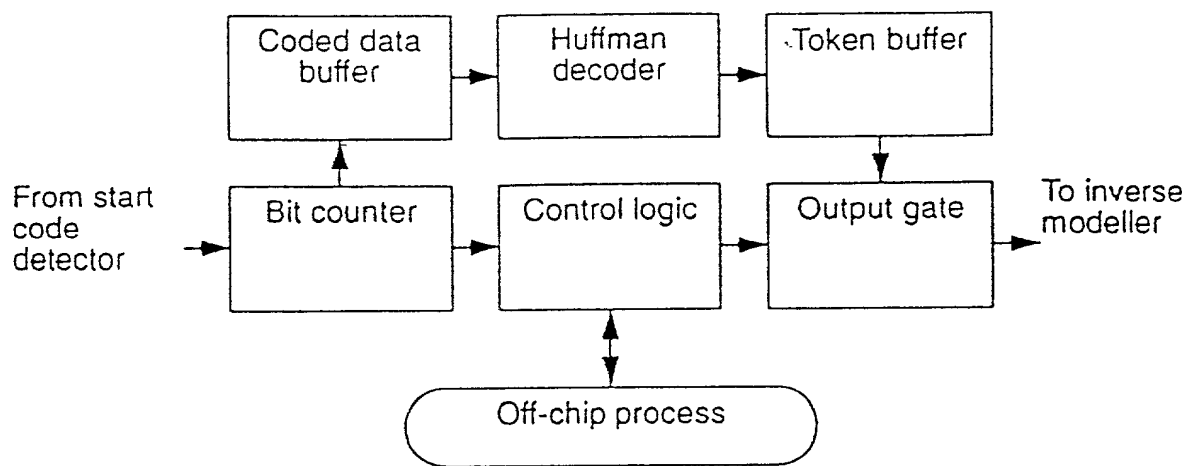


FIG. 68

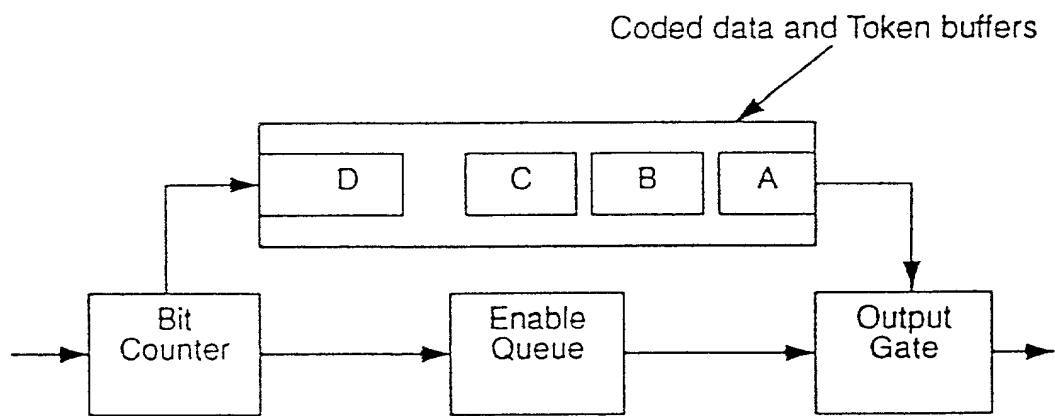


FIG. 69

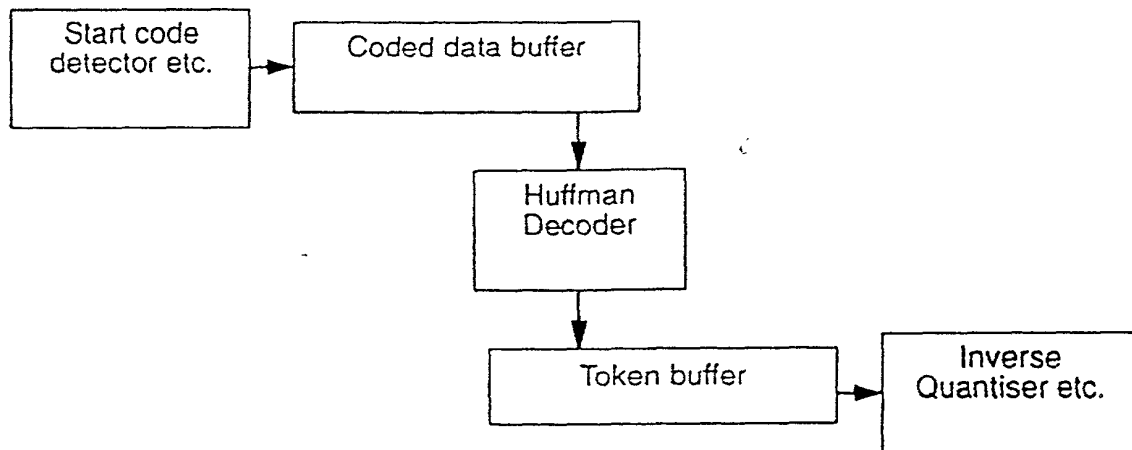


FIG.70

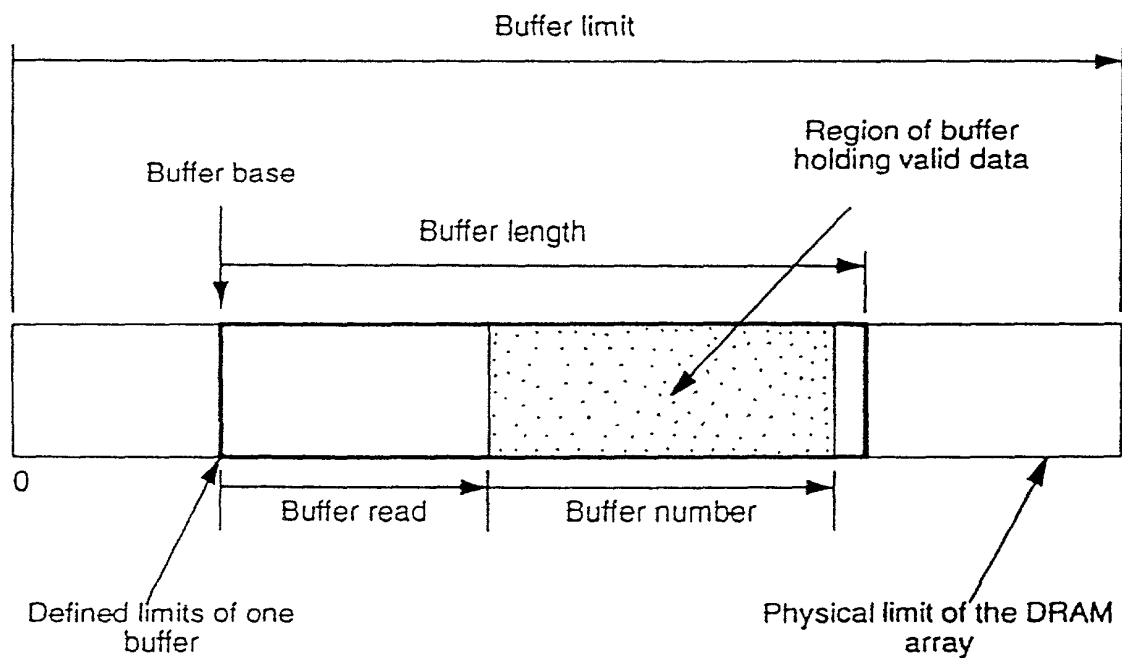


FIG.71

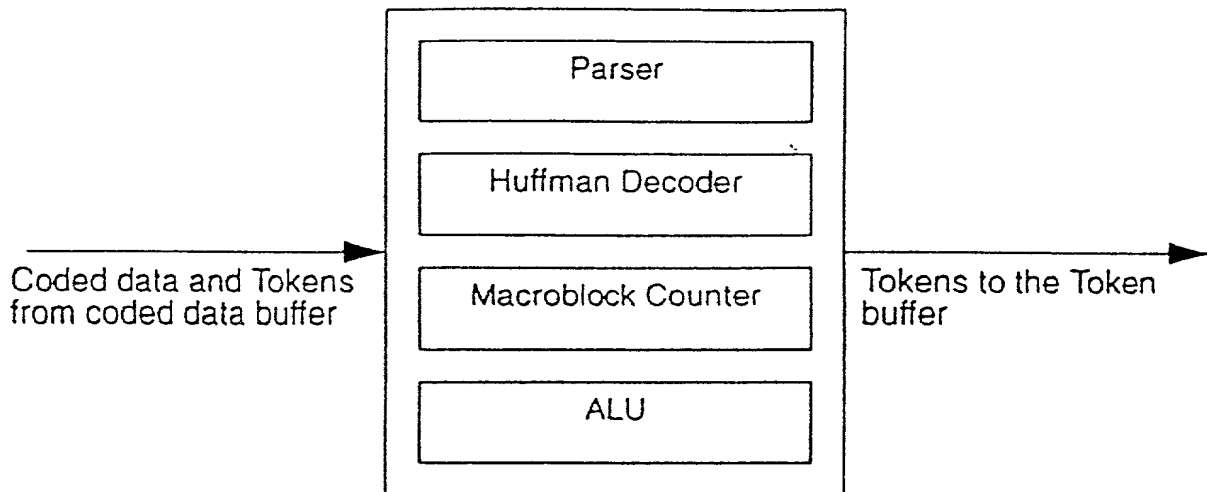


FIG.72

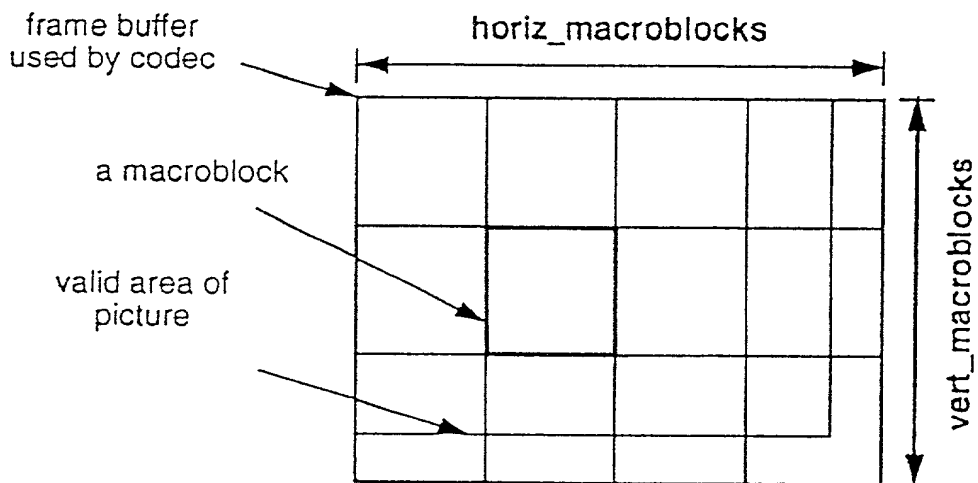


FIG.73

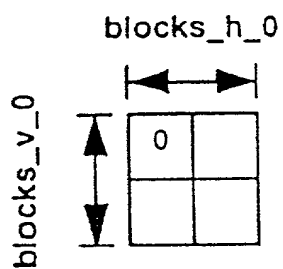


FIG.74A

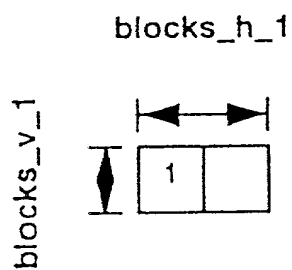


FIG.74B

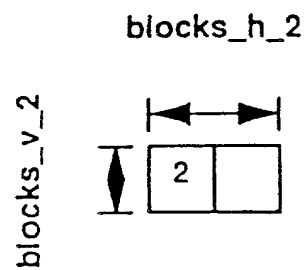


FIG.74C

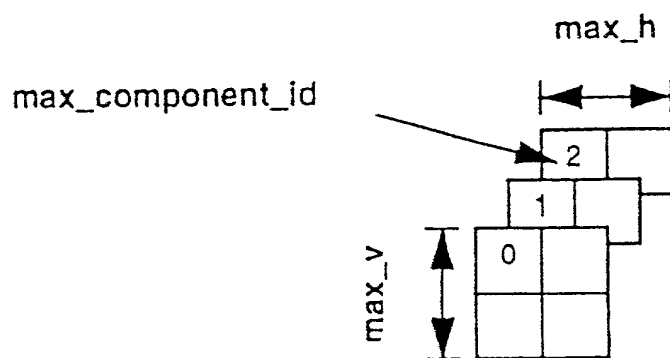


FIG.74D

$$\left\{ \begin{array}{l} \text{horiz_macroblocks} = \frac{\text{horiz_pels} + 15}{16} \\ \text{vert_macroblocks} = \frac{\text{vert_pels} + 15}{16} \end{array} \right.$$

FIG.75

From Token buffer

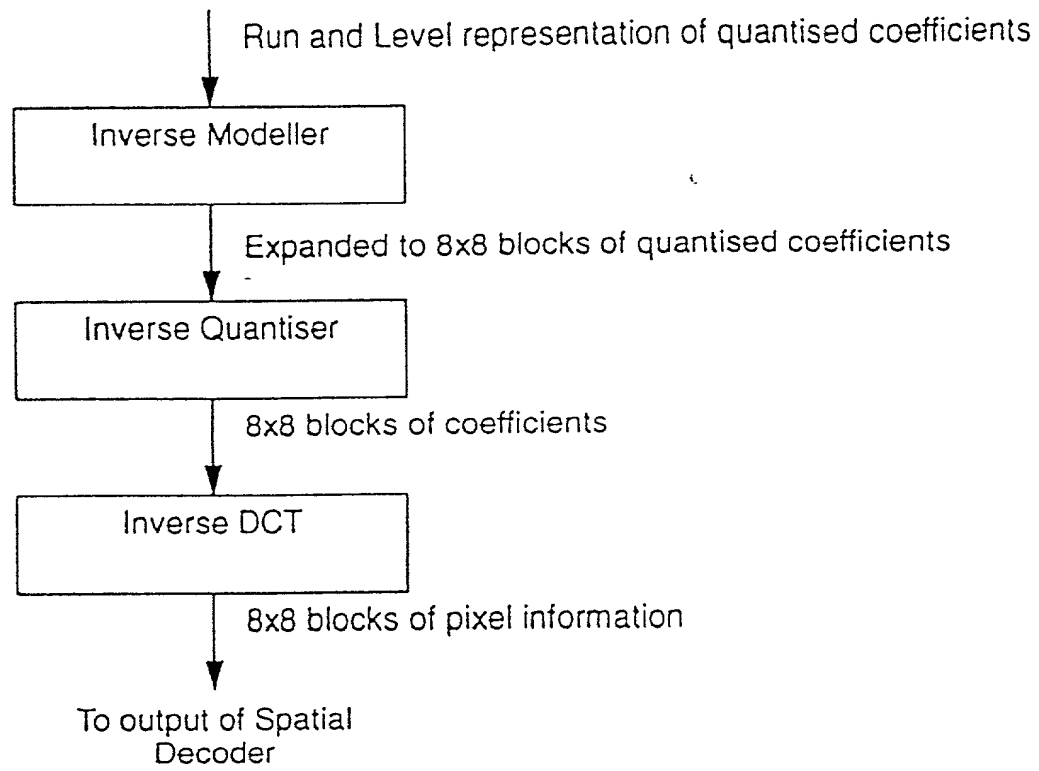


FIG.76

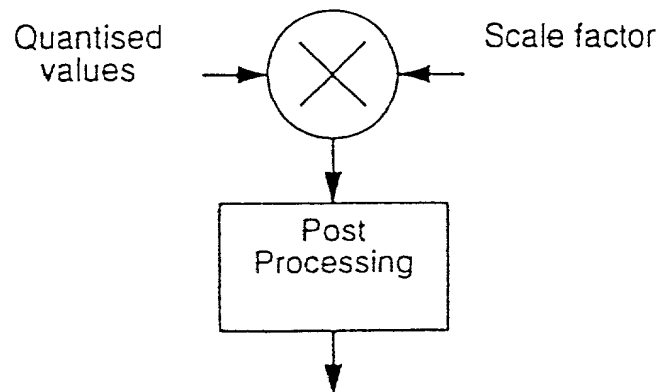


FIG.77

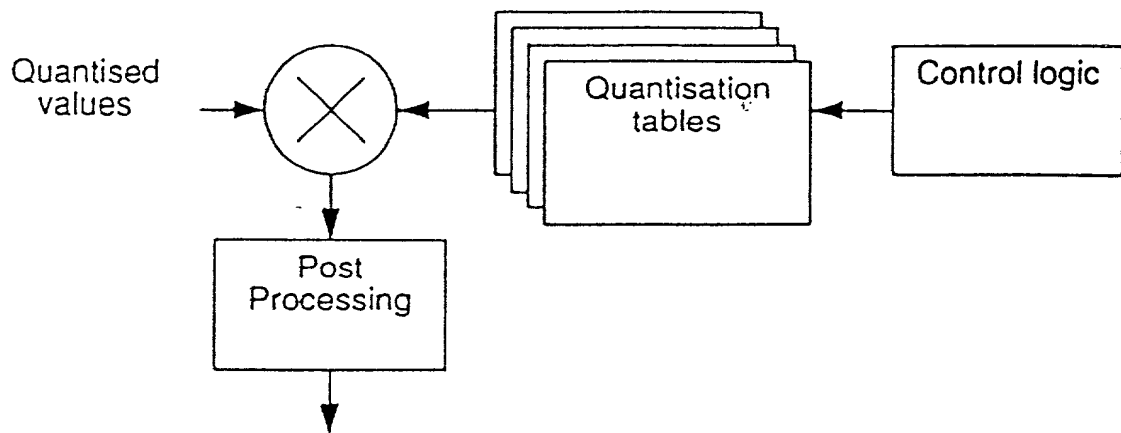


FIG.78

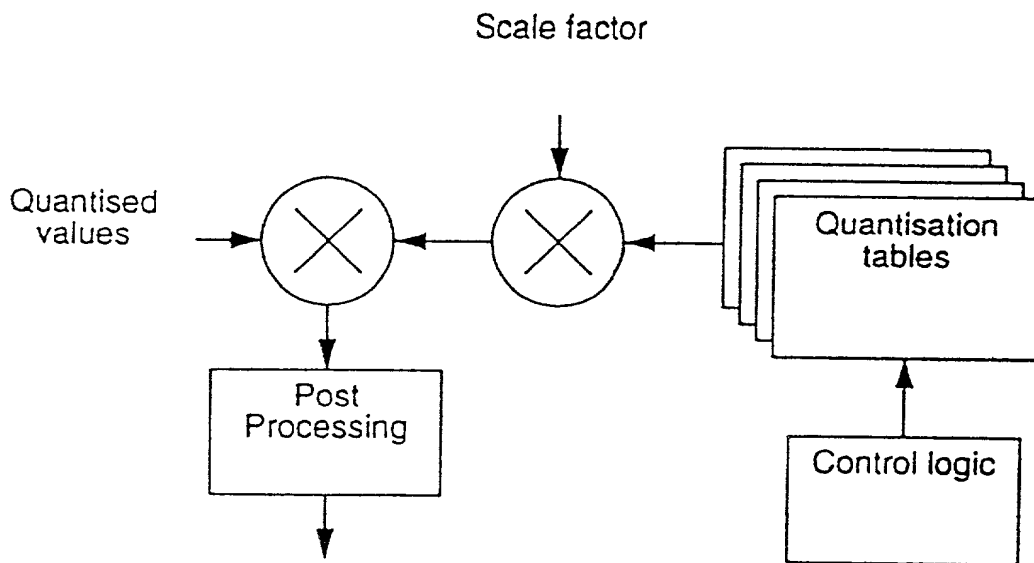


FIG.79

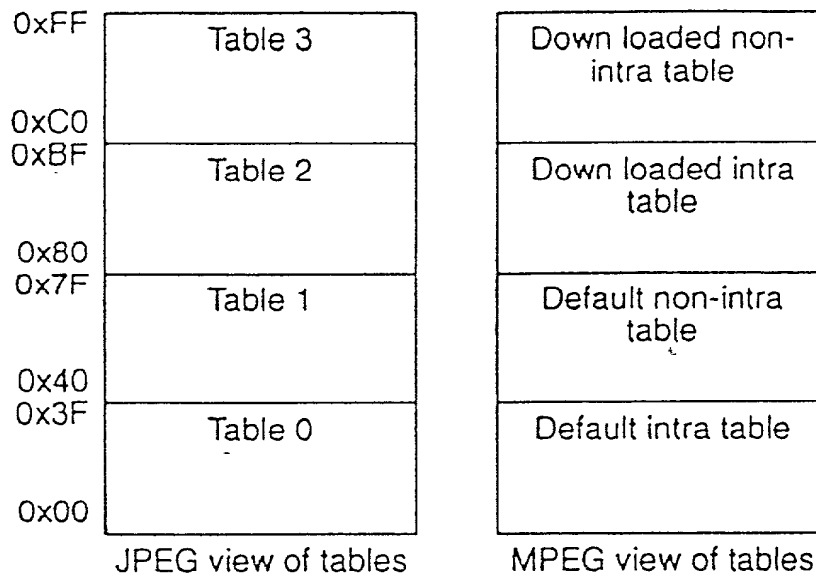


FIG.80

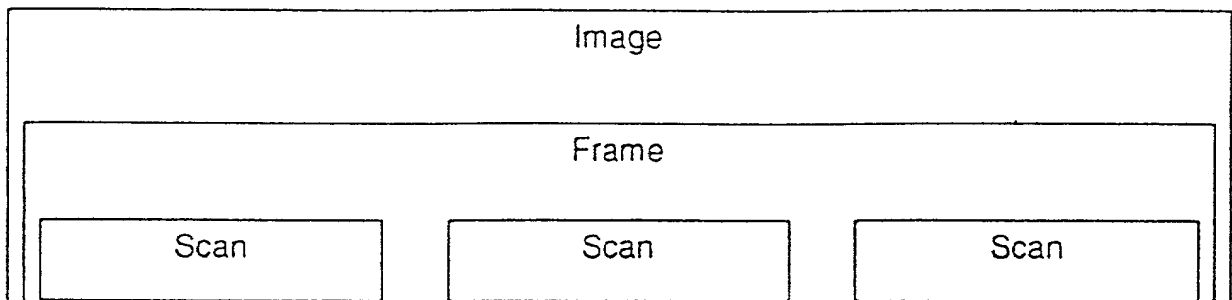


FIG.8 1

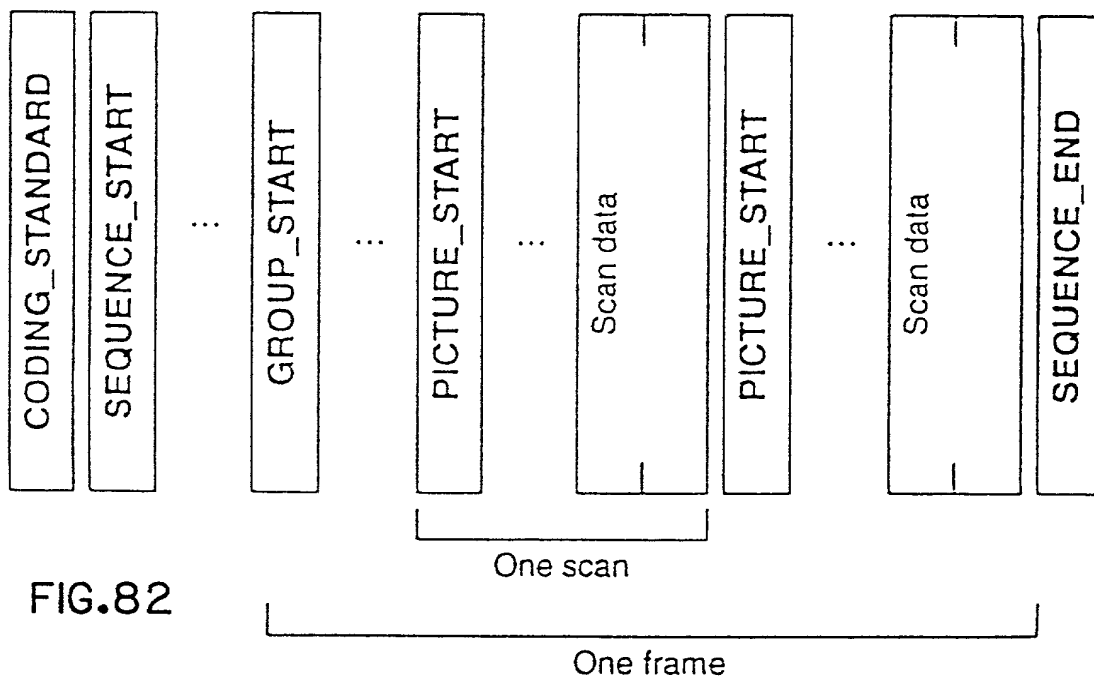


FIG.82

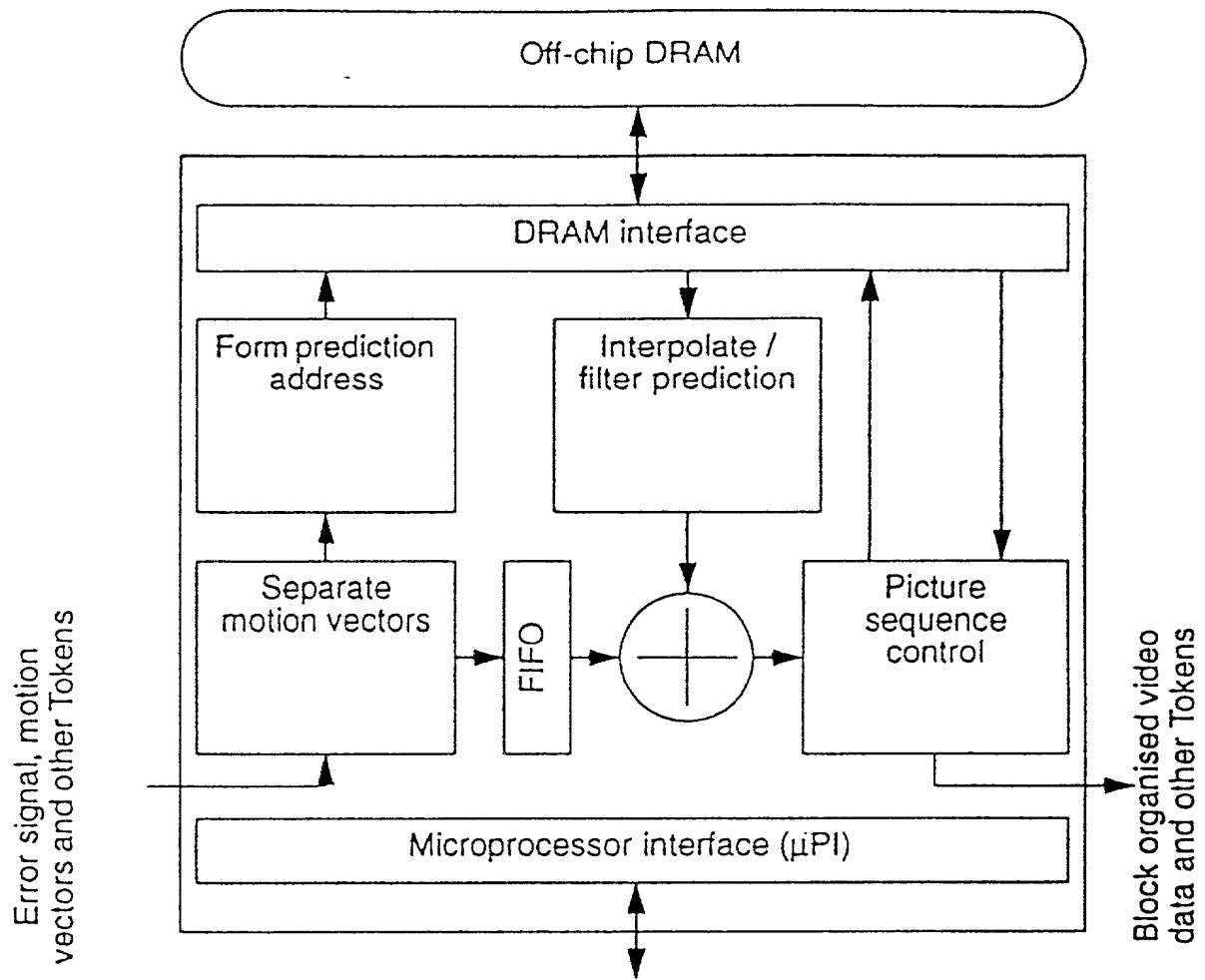


FIG.83

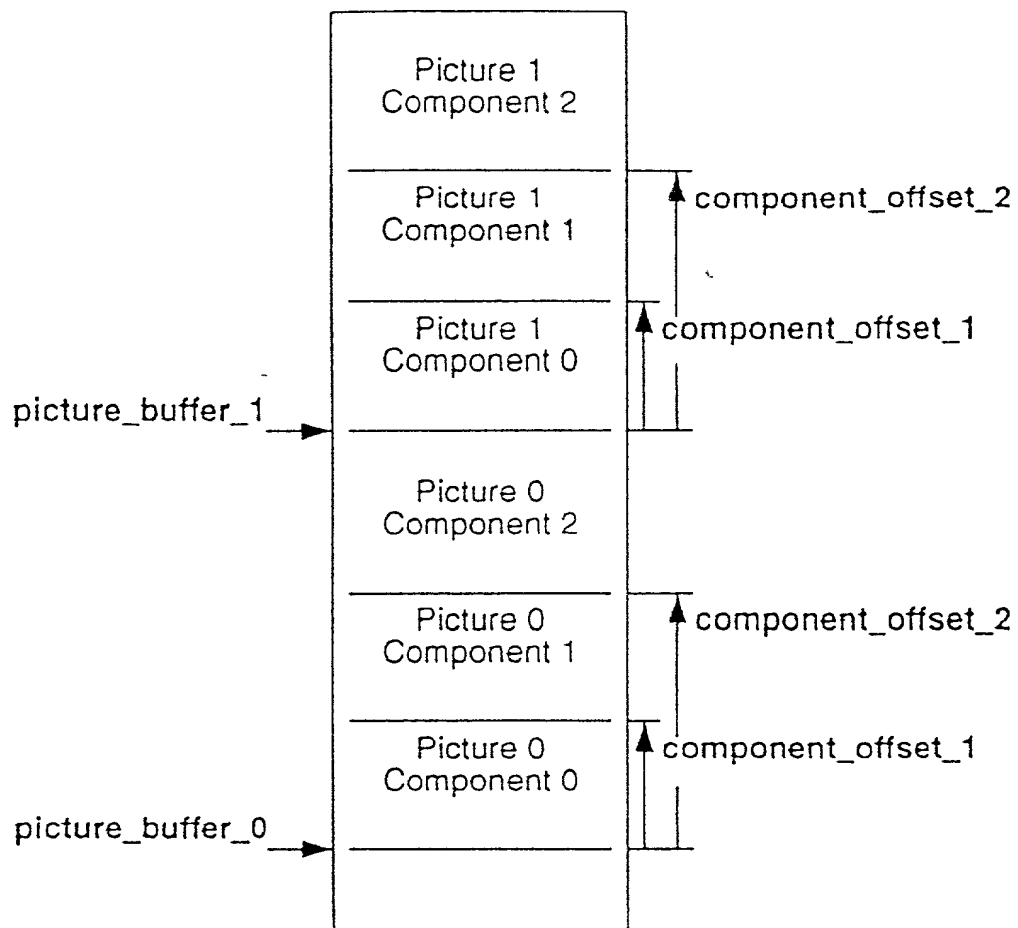


FIG.84

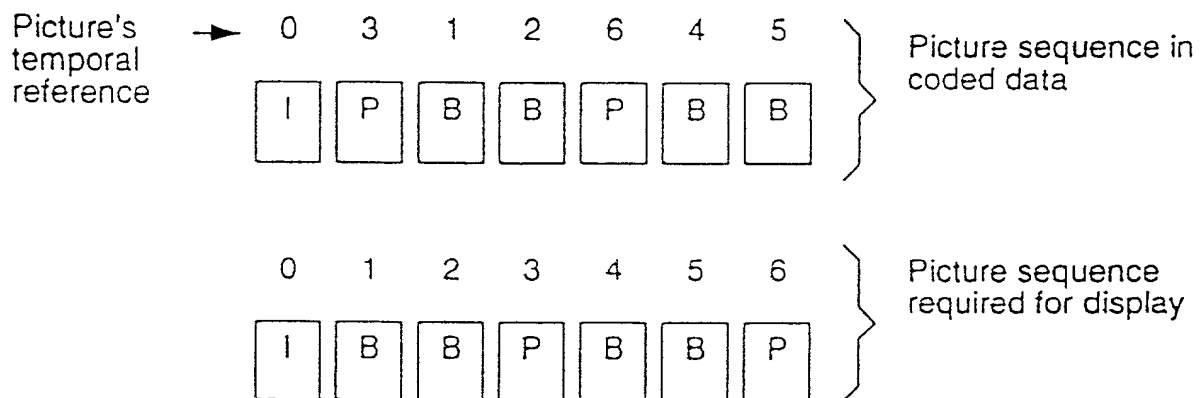


FIG.85

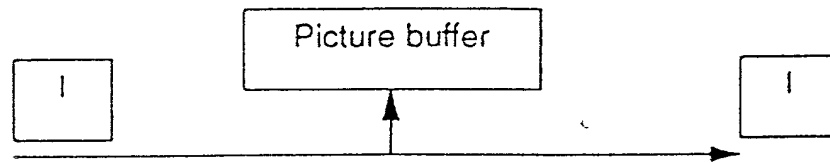


FIG.86

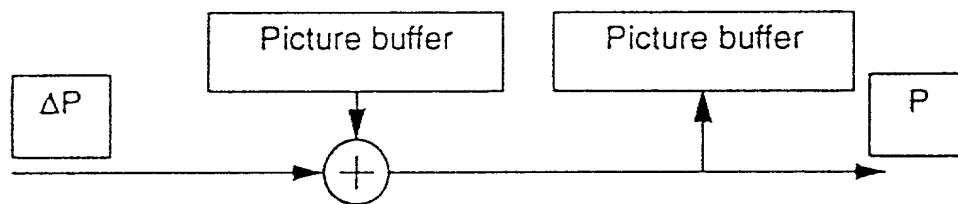


FIG.87

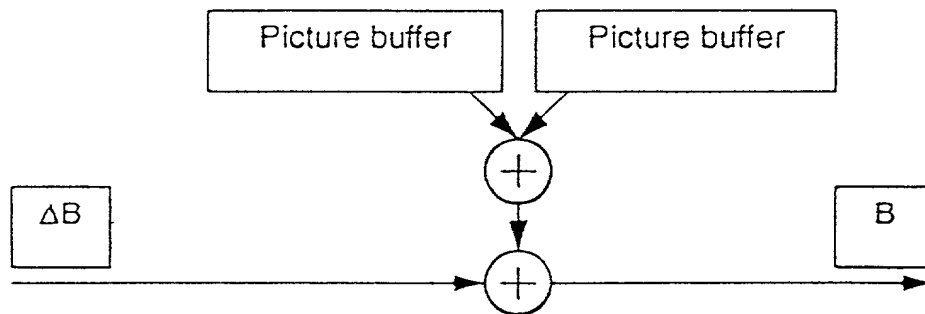


FIG.88

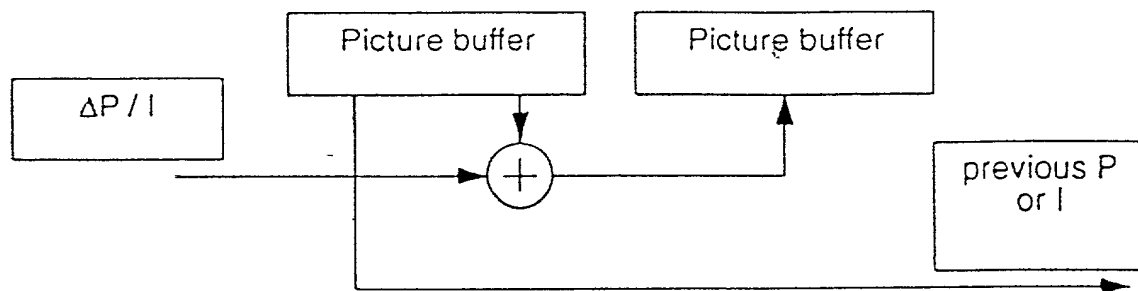


FIG.89

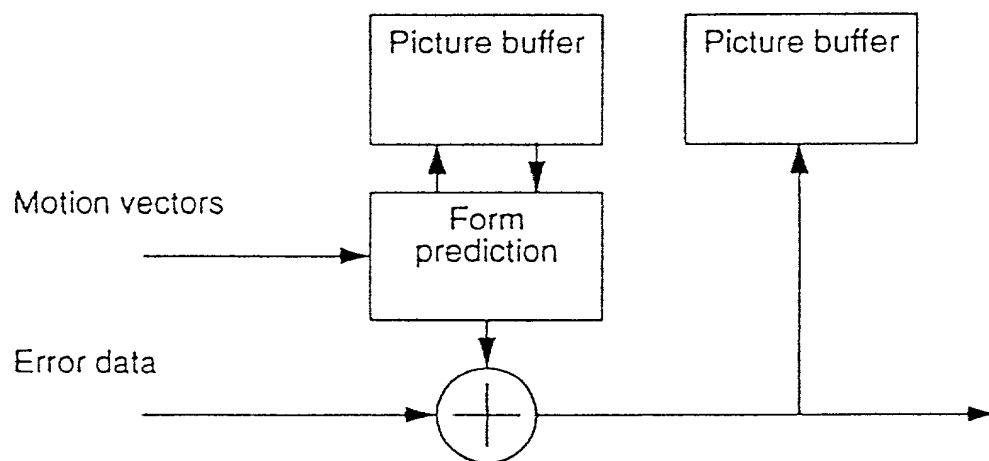


FIG.90

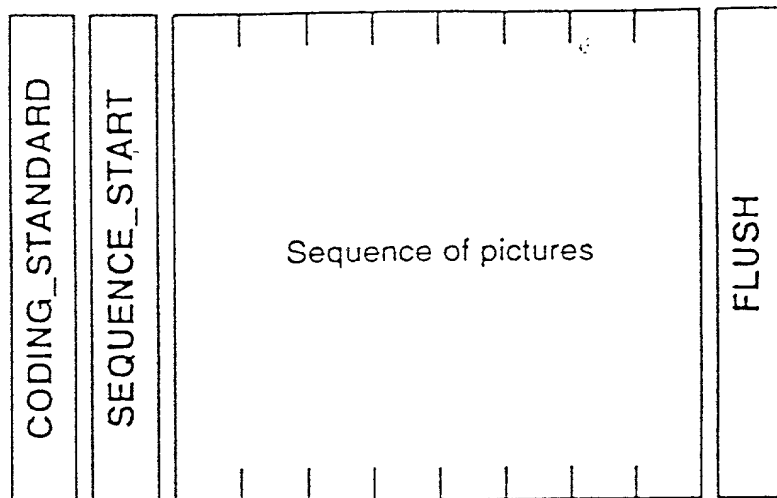


FIG.91

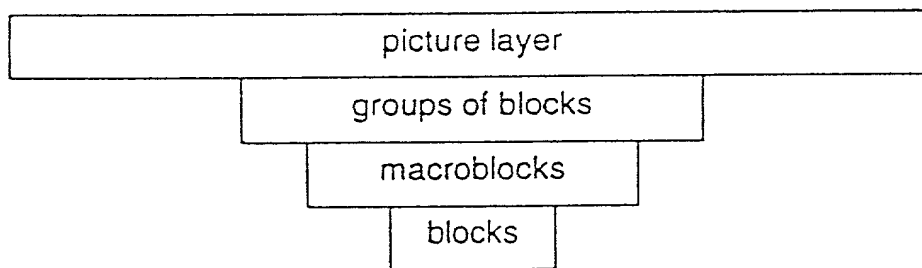


FIG.92

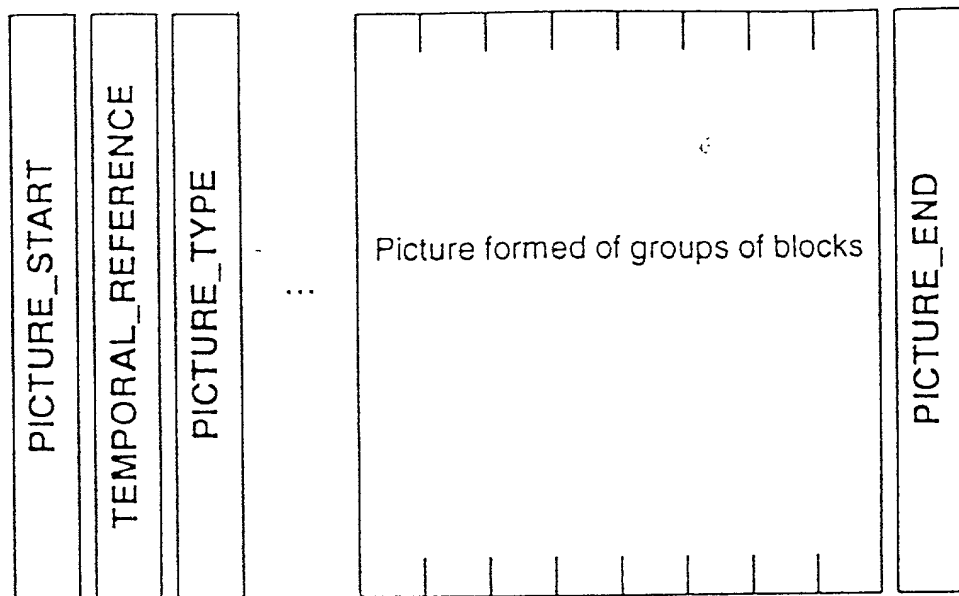


FIG.93

CIF		QCIF	
0	1	0	
2	3	2	
4	5	4	
6	7		
8	9		
10	11		

FIG.94

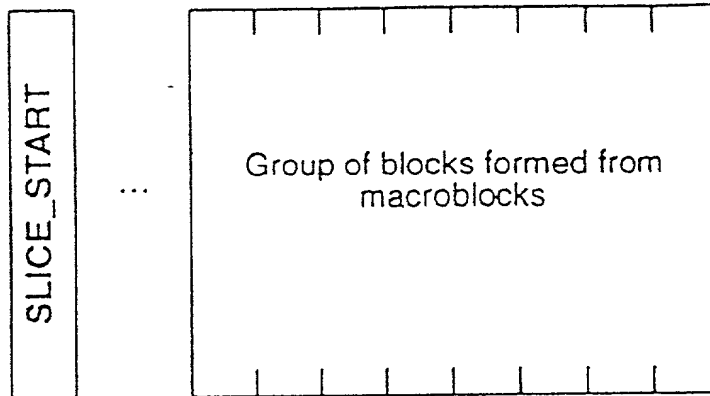


FIG.95

1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22
23	24	25	26	27	28	29	30	31	32	33

FIG.96

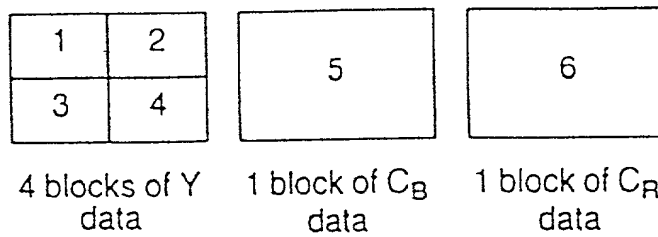


FIG.97

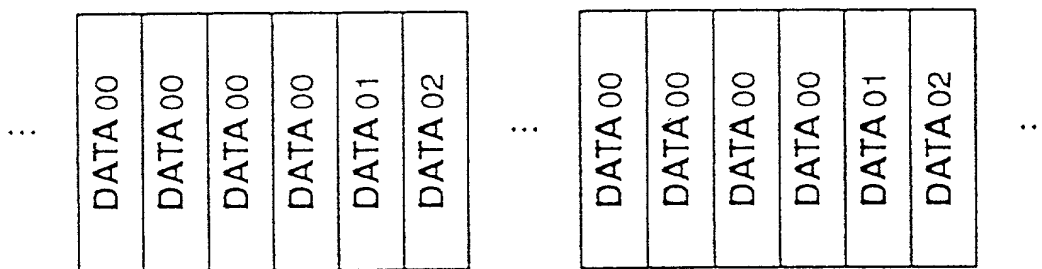


FIG.98

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16

⋮

59	58	59	60	61	62	63	64
----	----	----	----	----	----	----	----

FIG.99

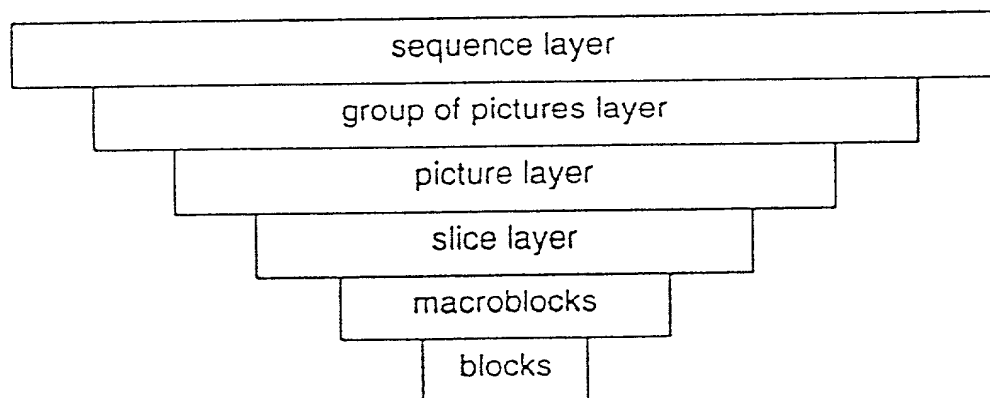


FIG. 100

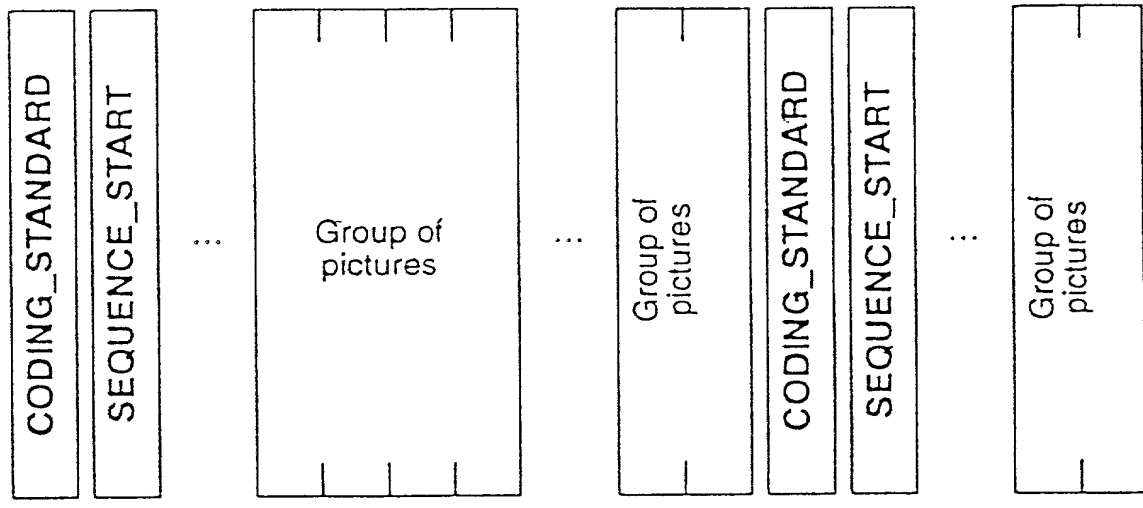


FIG. 101

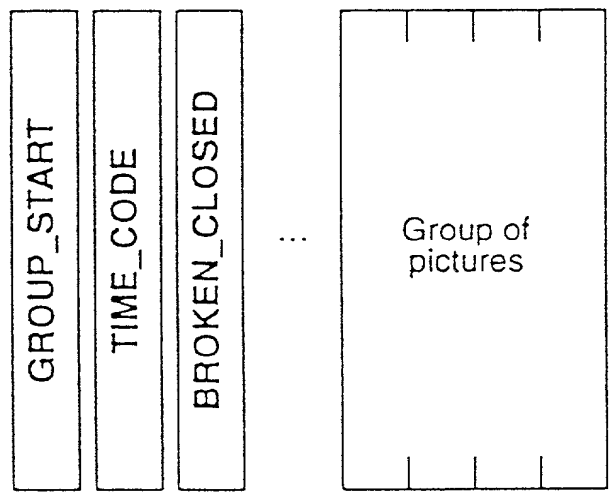


FIG. 102

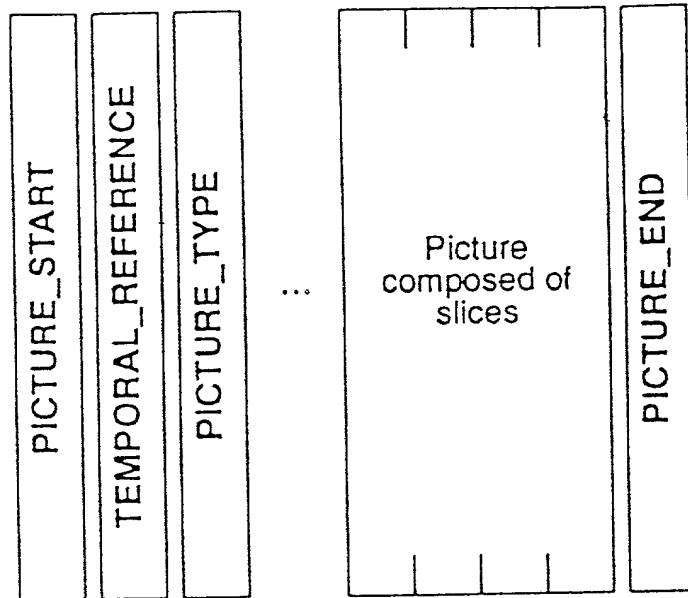


FIG. 103

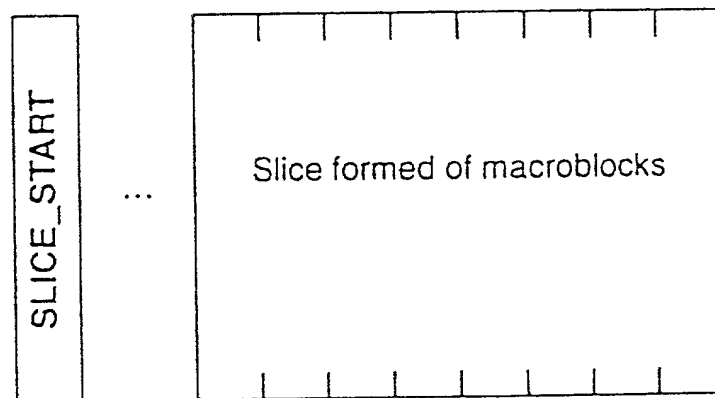


FIG. 104

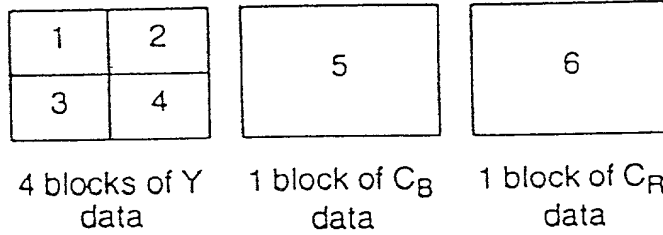


FIG. 105

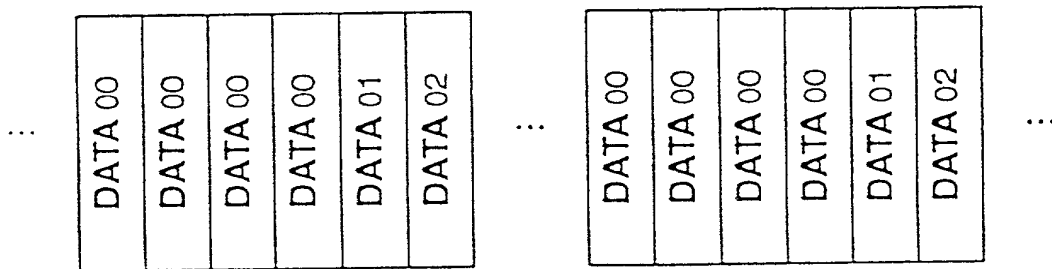


FIG. 106

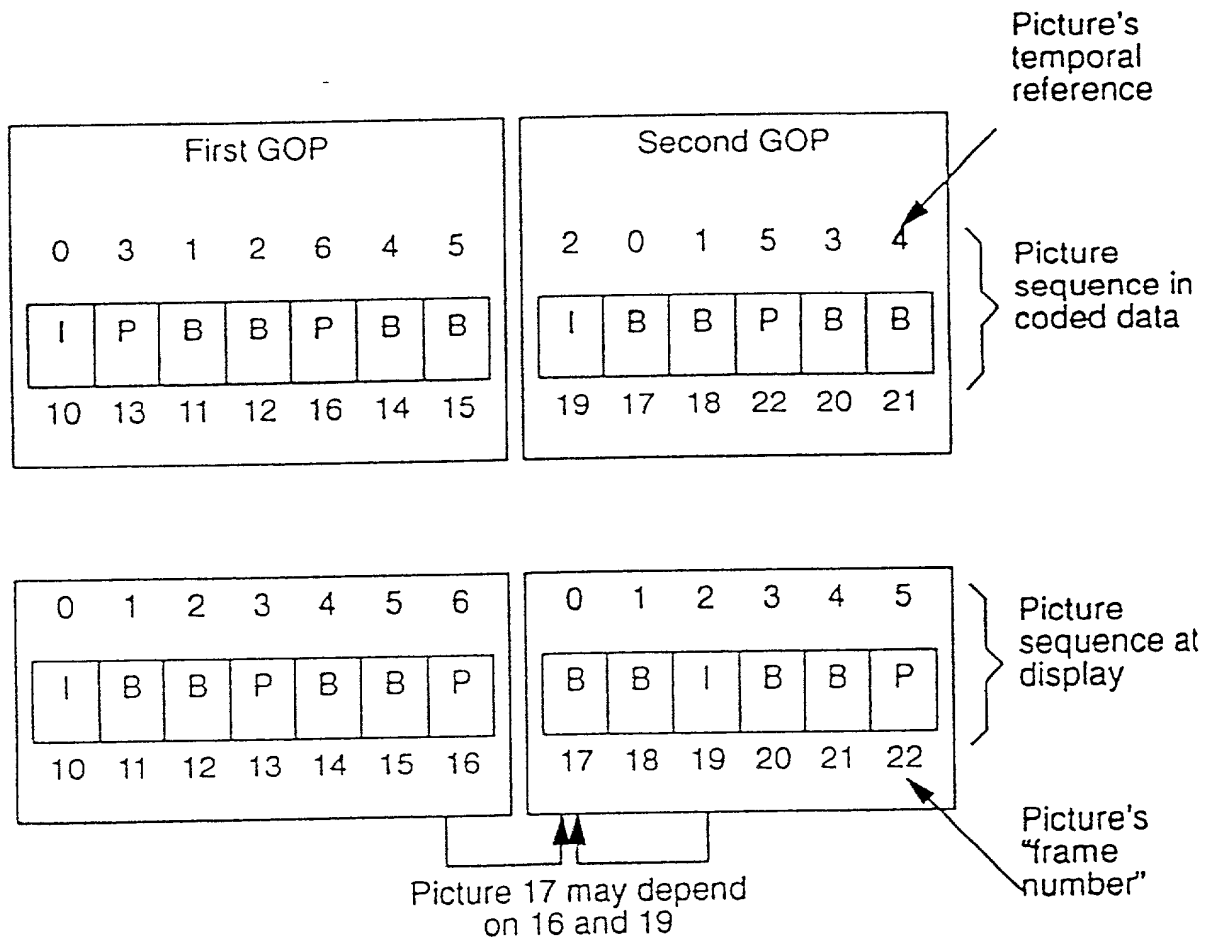


FIG. 107

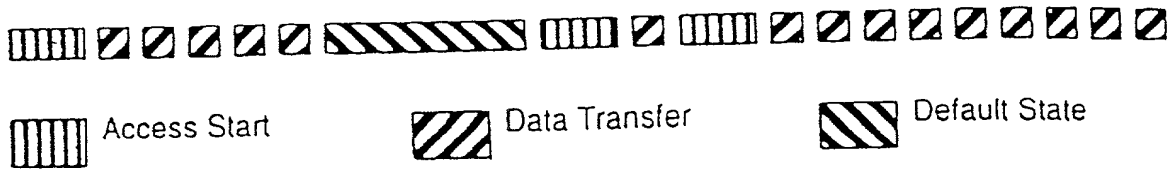


FIG. 108

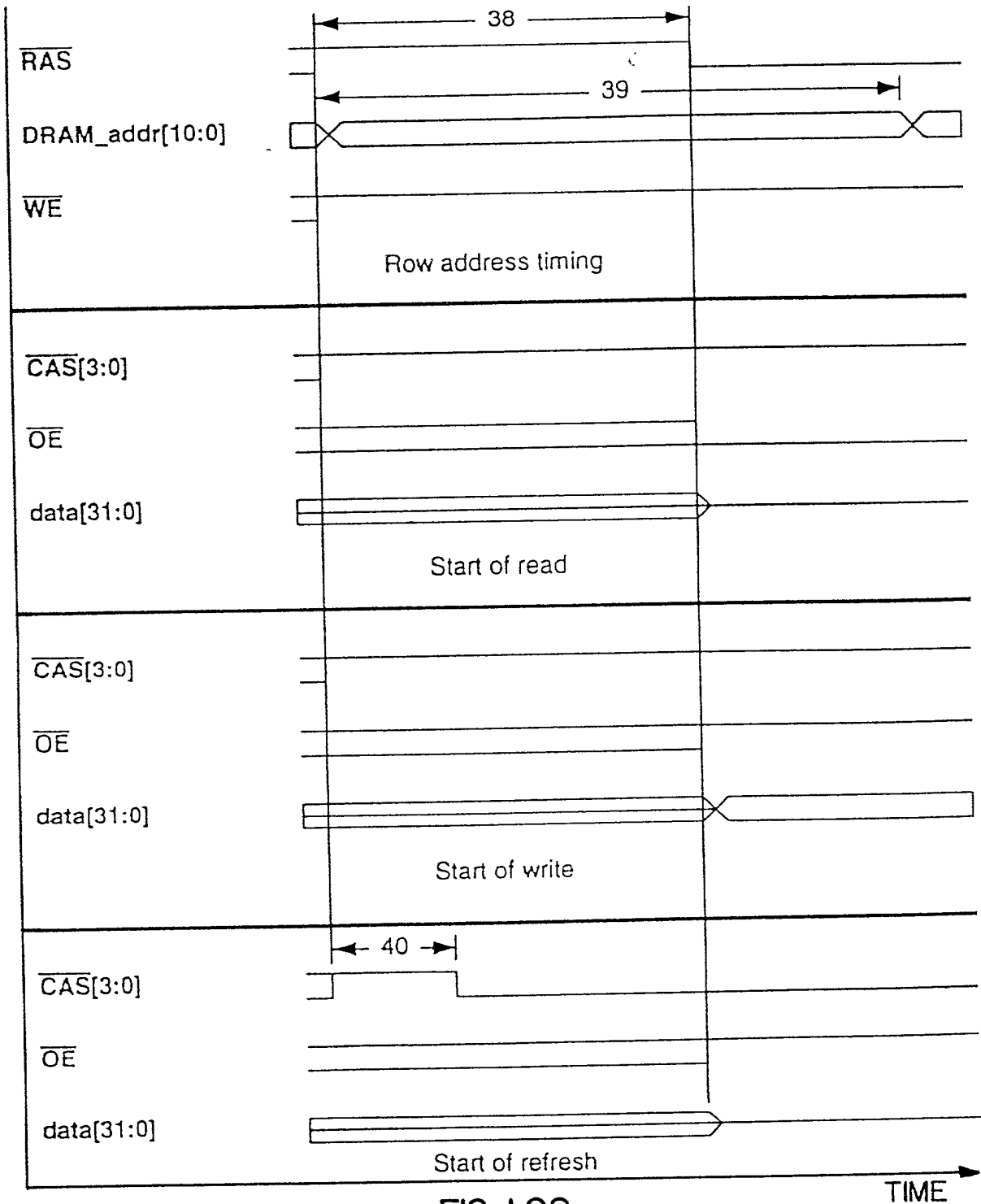


FIG. 109

$\overline{\text{RAS}}$

DRAM_addr[10:0]

$\overline{\text{CAS}}[3:0]$

$\overline{\text{WE}}$

$\overline{\text{OE}}$

DRAM_data[31:0]

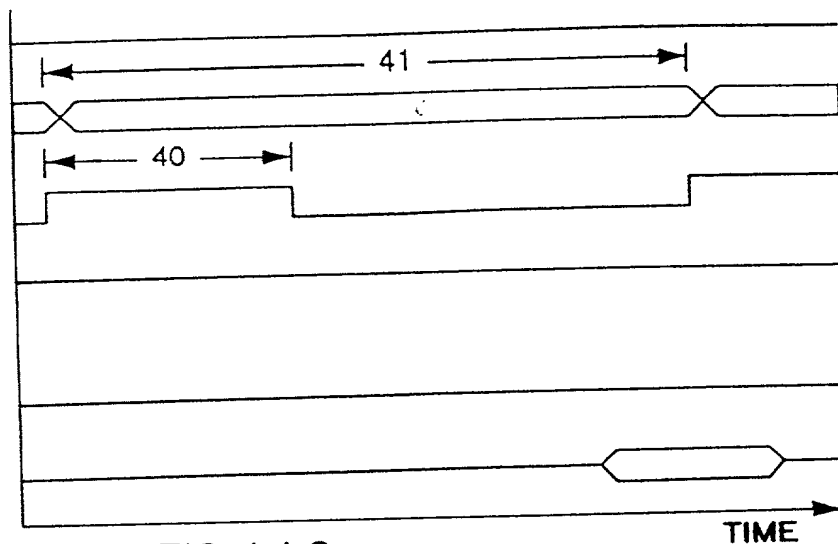


FIG. 110

$\overline{\text{RAS}}$

DRAM_addr[10:0]

$\overline{\text{CAS}}[3:0]$

$\overline{\text{WE}}$

$\overline{\text{OE}}$

DRAM_data[31:0]

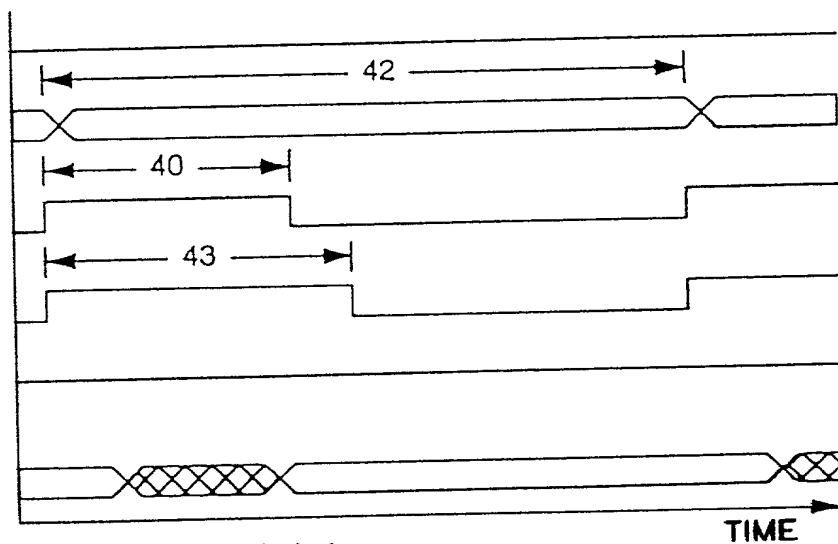


FIG. 111

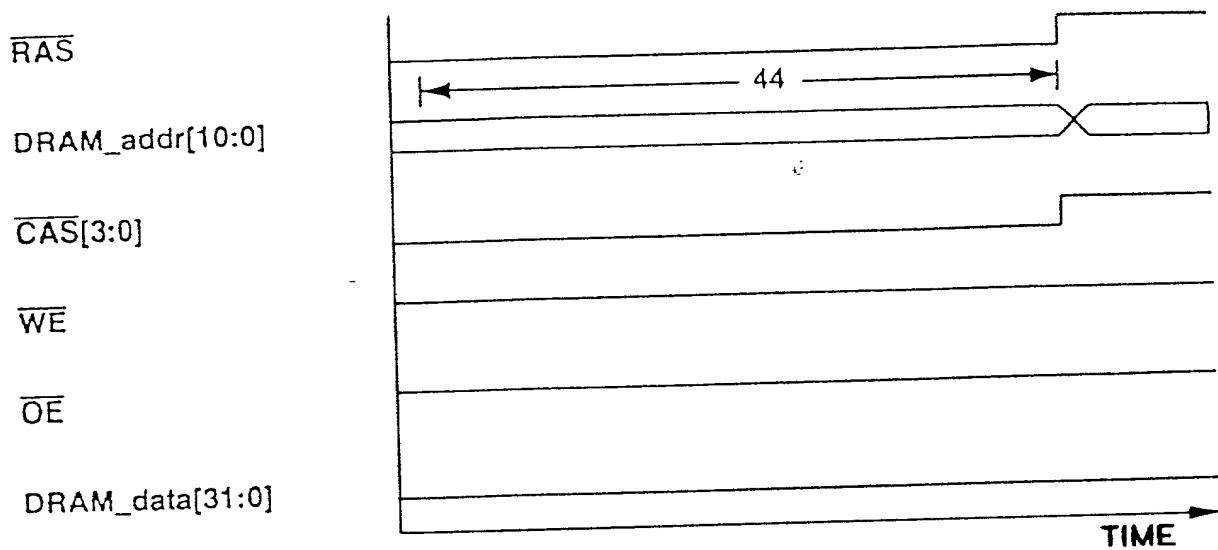


FIG. 112

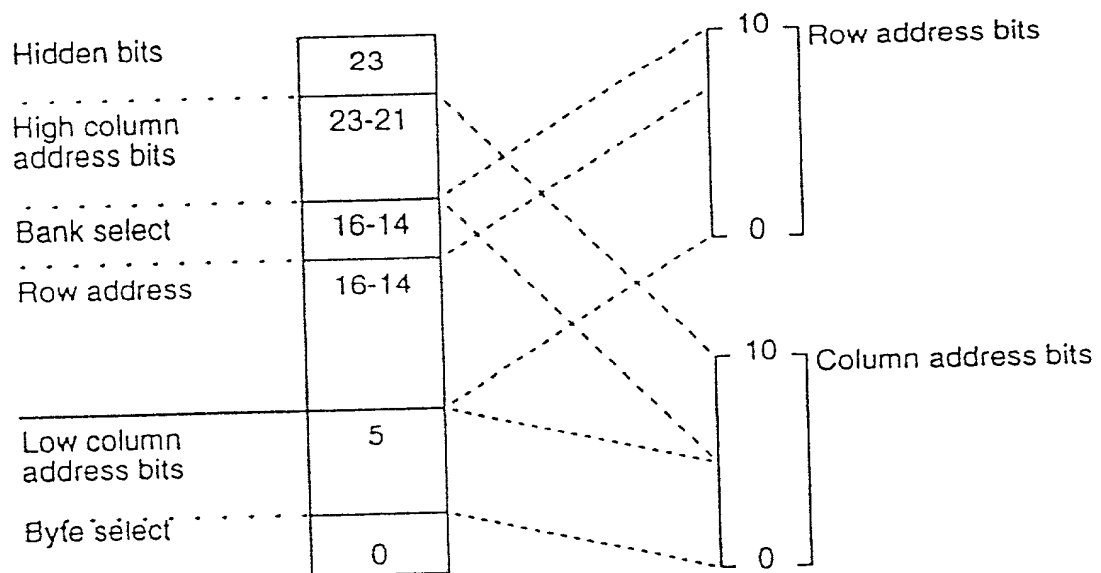


FIG. 113

Any signal

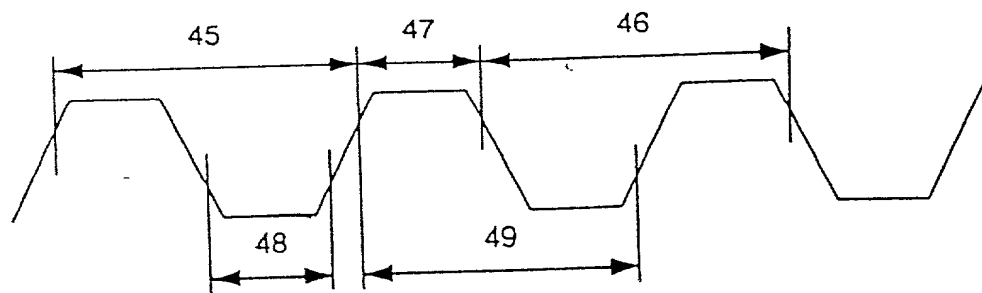


FIG. 114

Any signal

Any other
signal

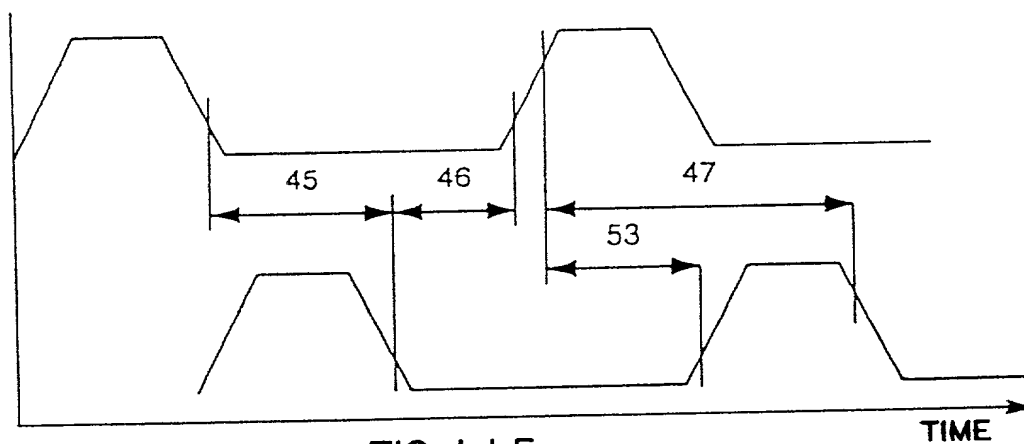


FIG. 115

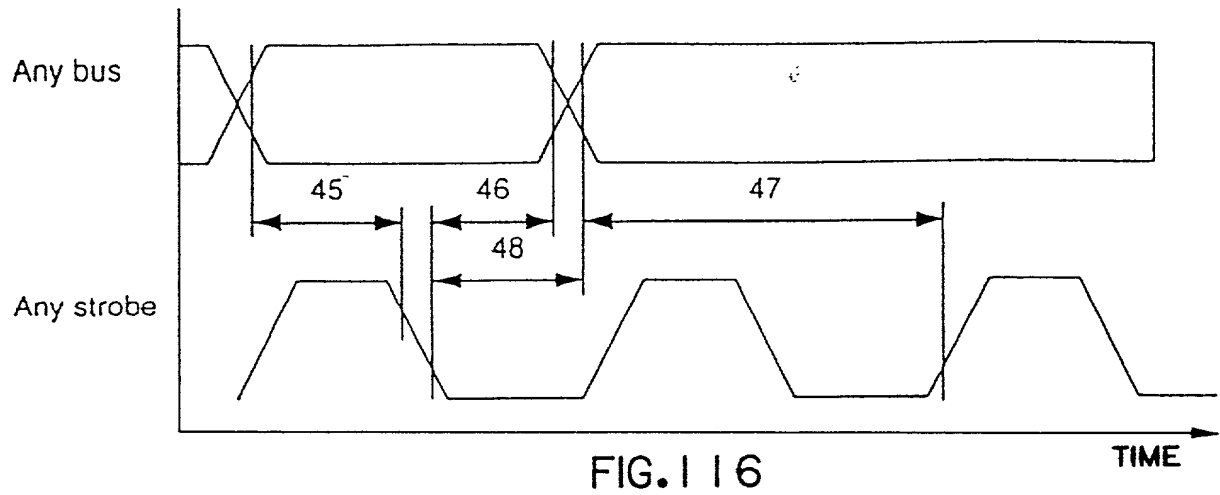


FIG. 116

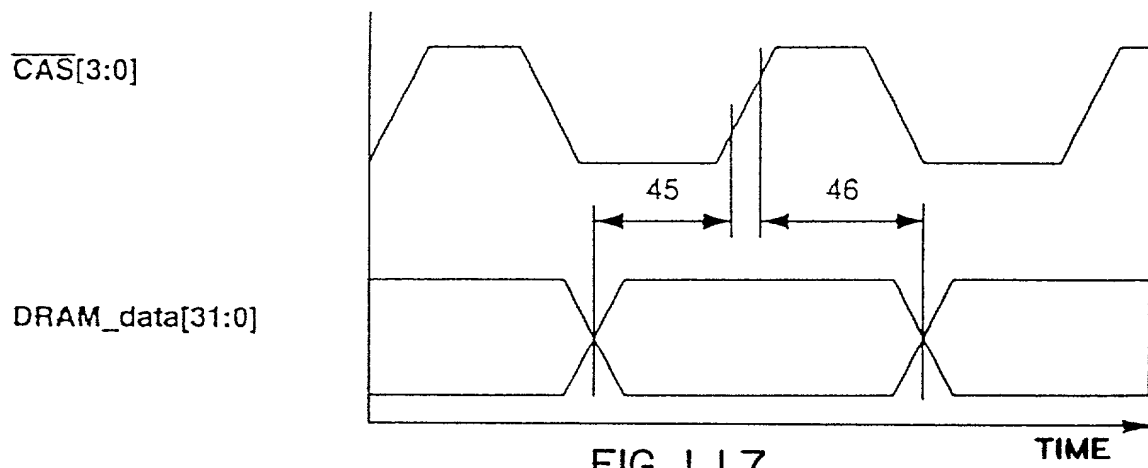


FIG. 117

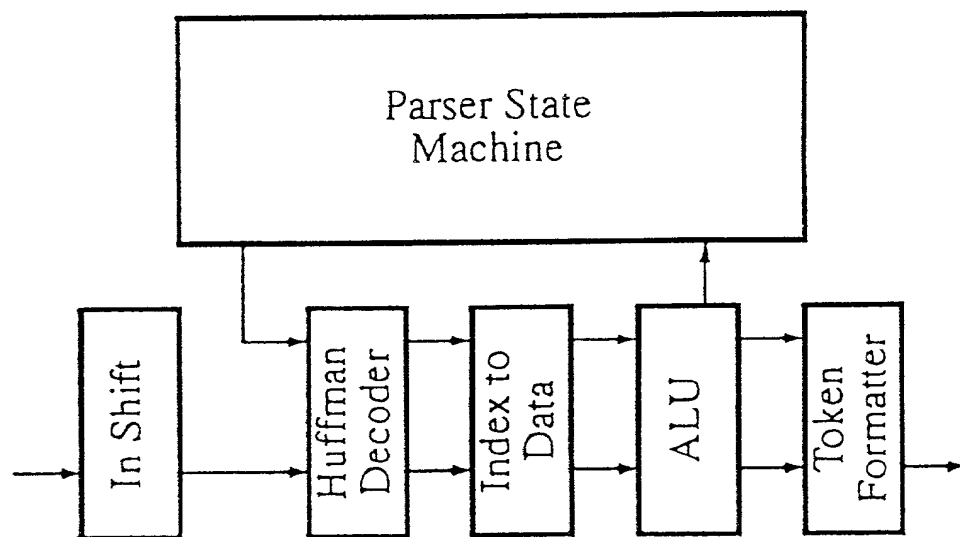


FIG. 118

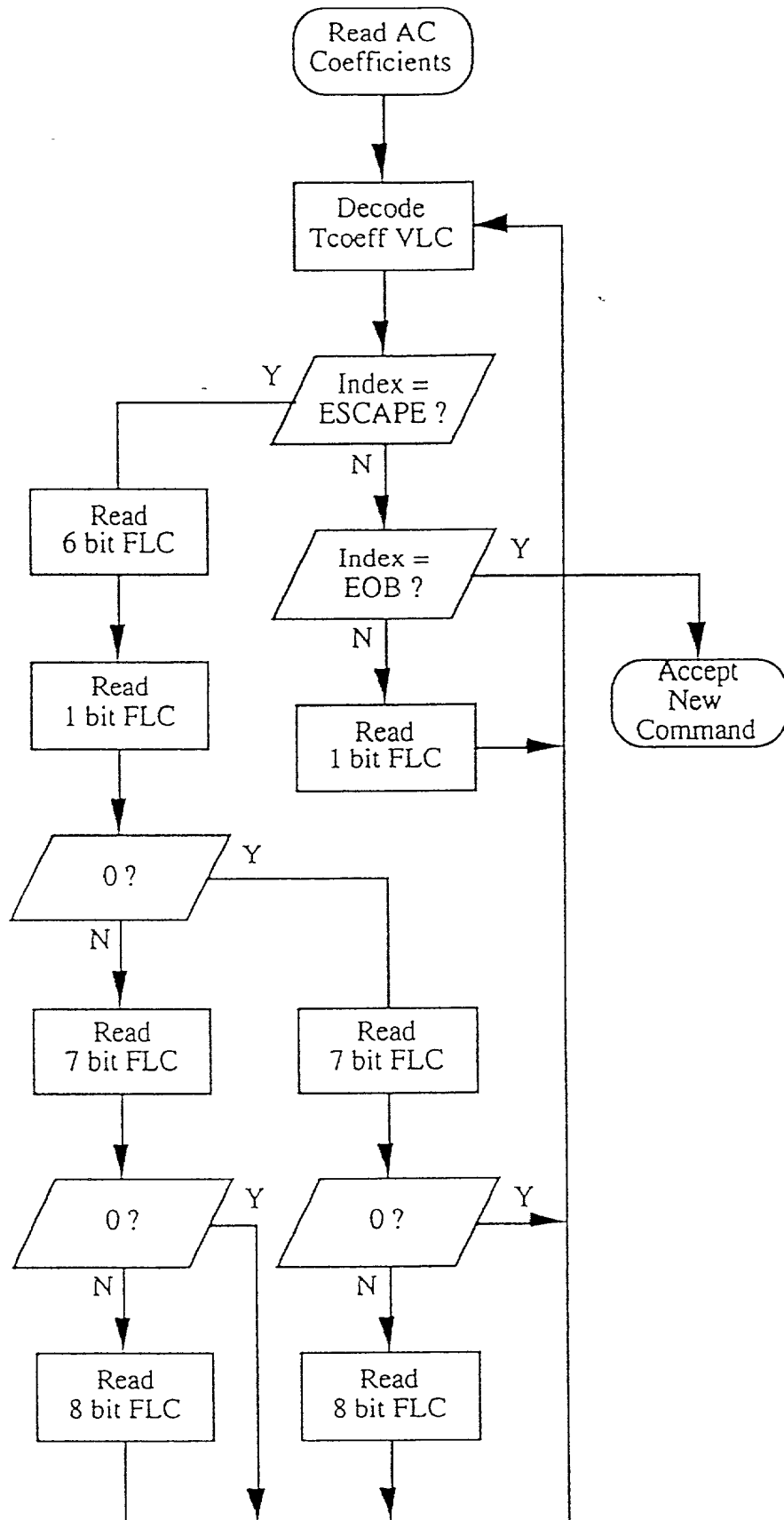


FIG. 119

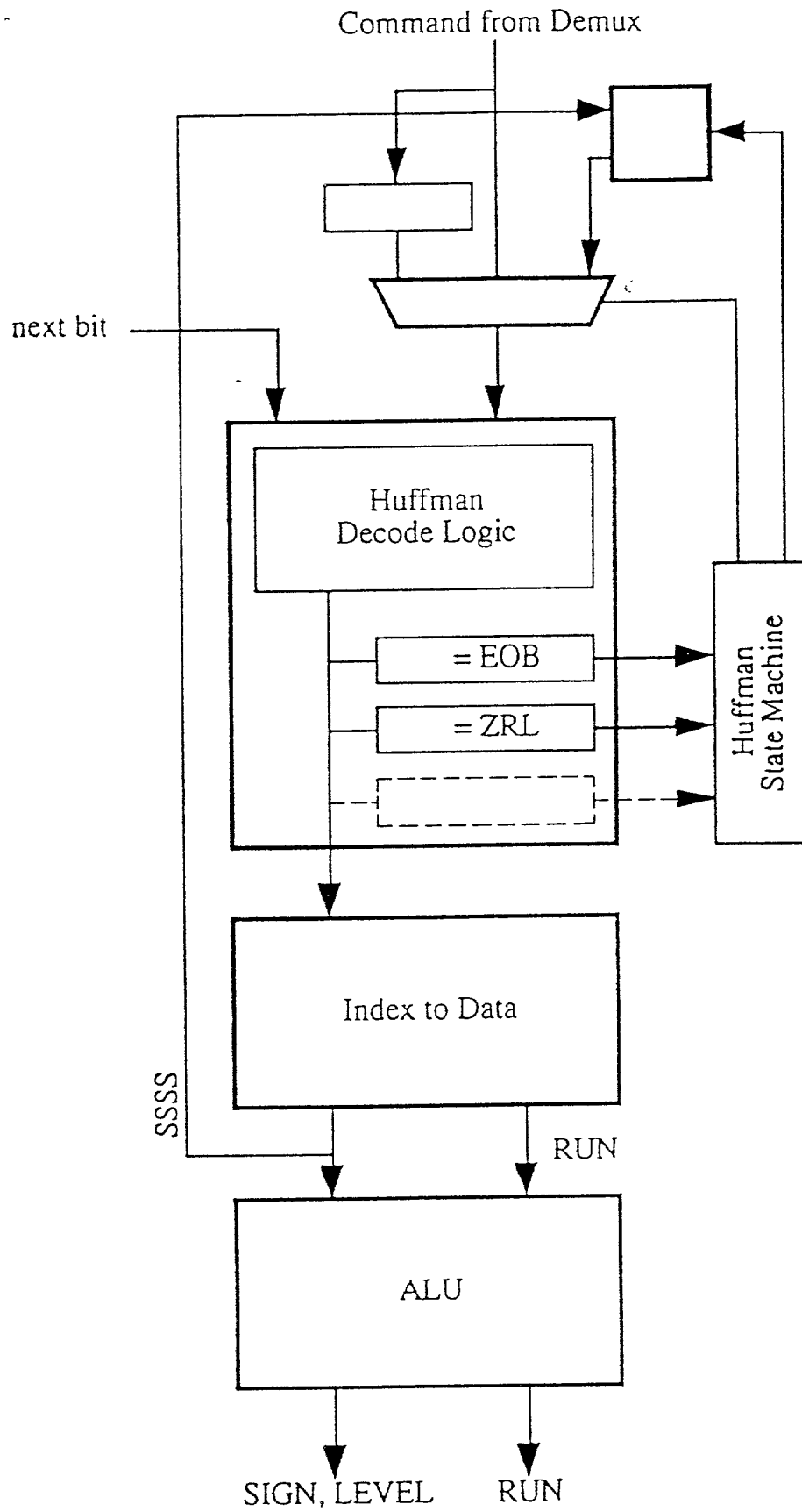


FIG. 120

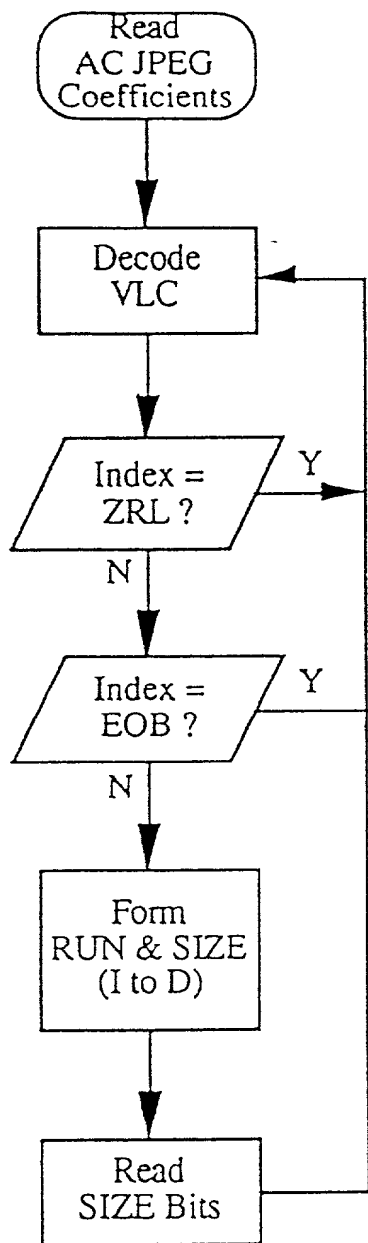


FIG. 121A

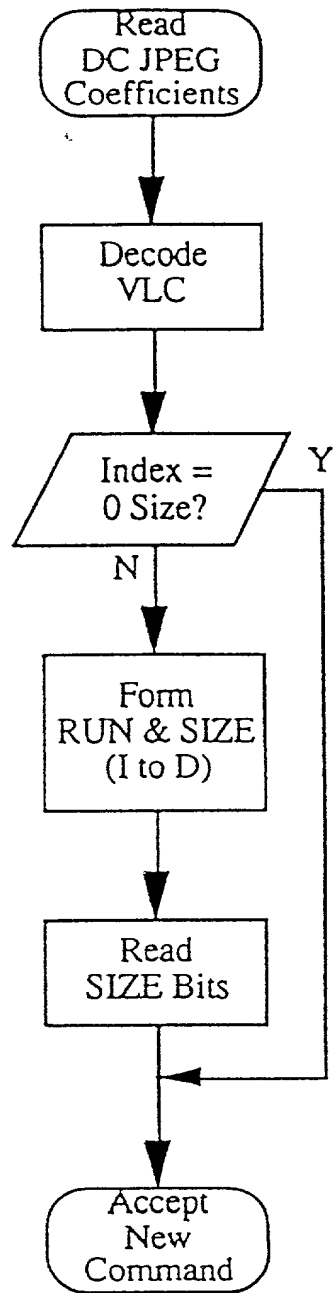


FIG. 121B

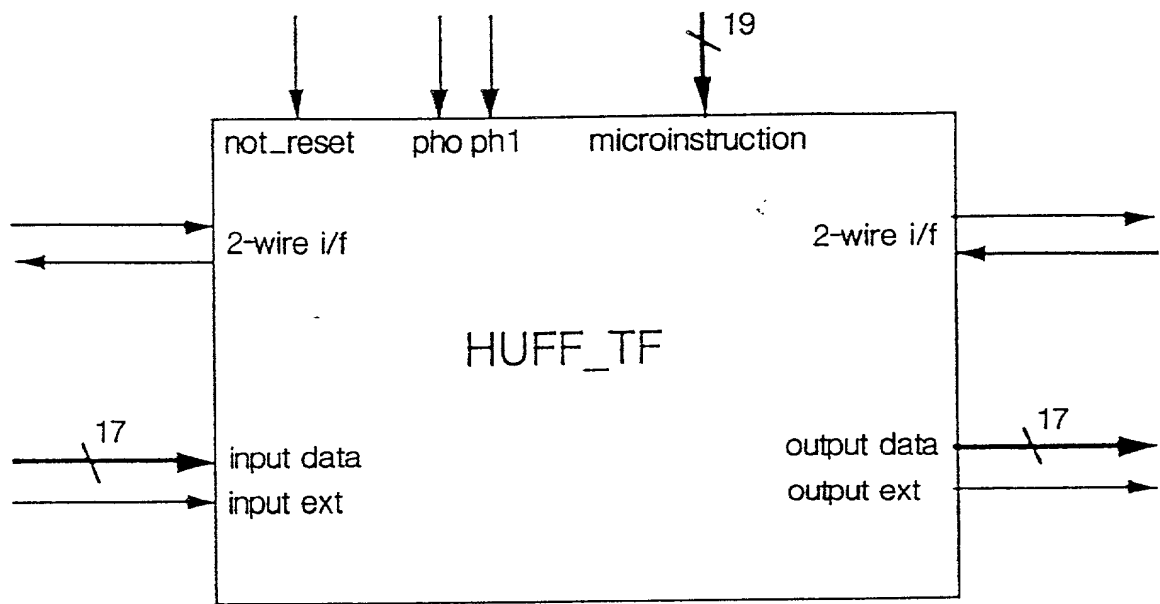


FIG. I 22

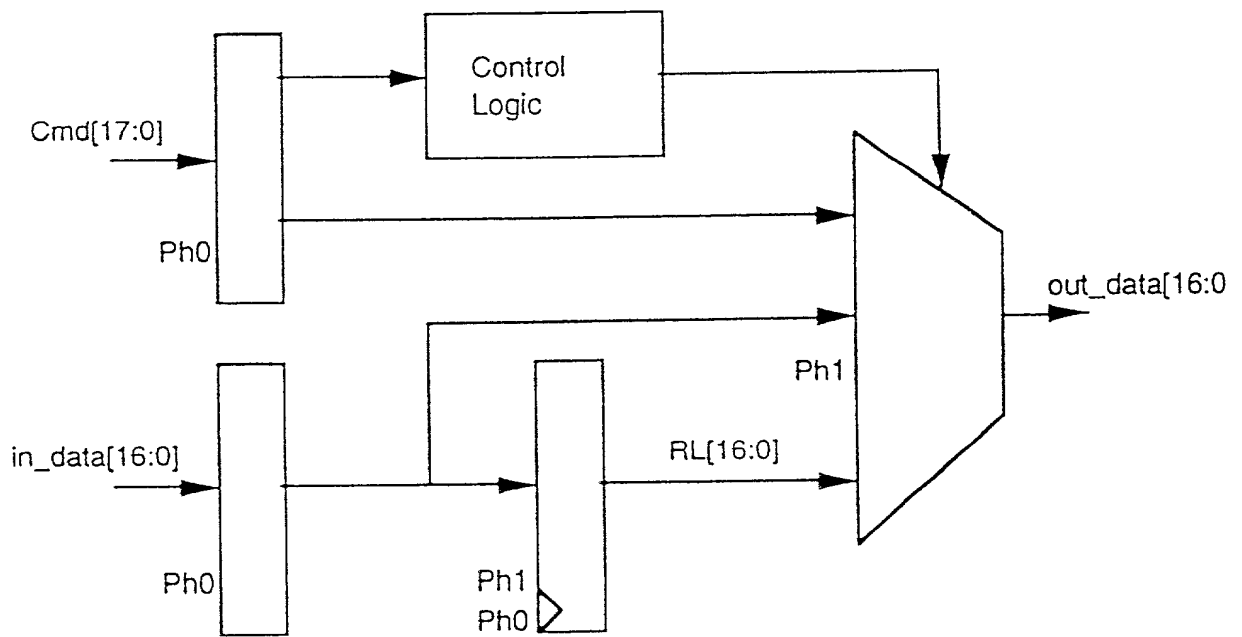


FIG. I 23

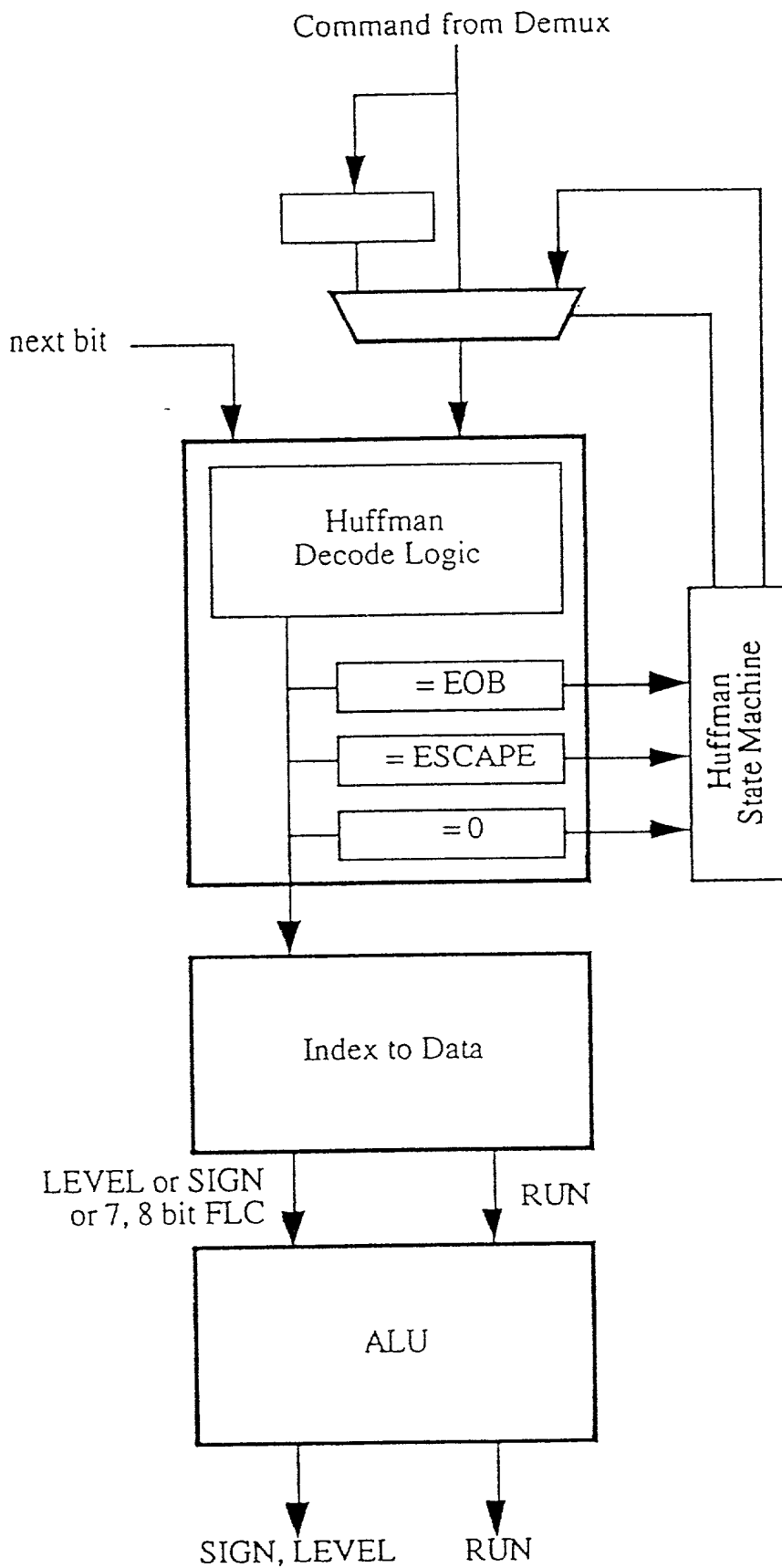


FIG. 124

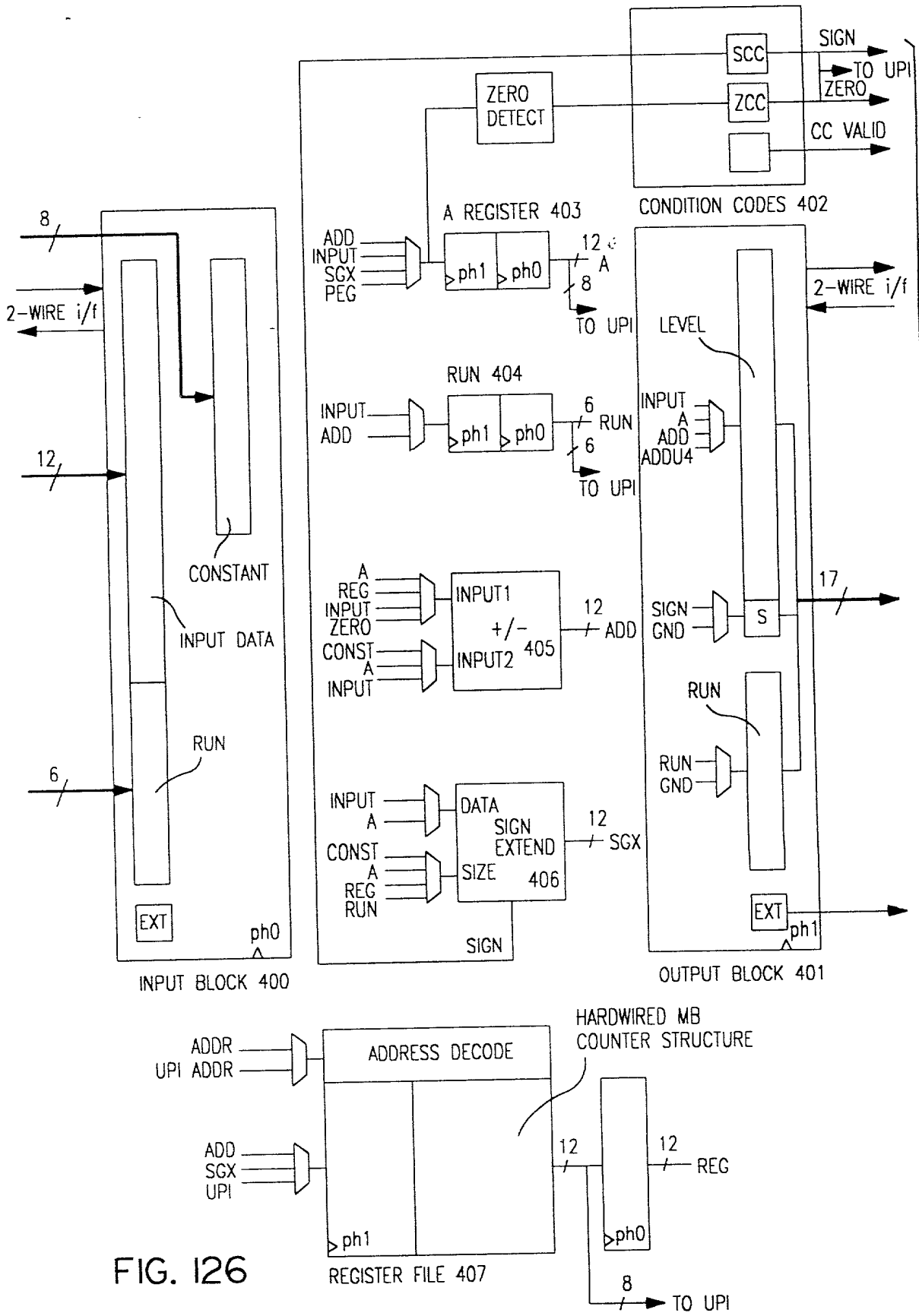


FIG. 126

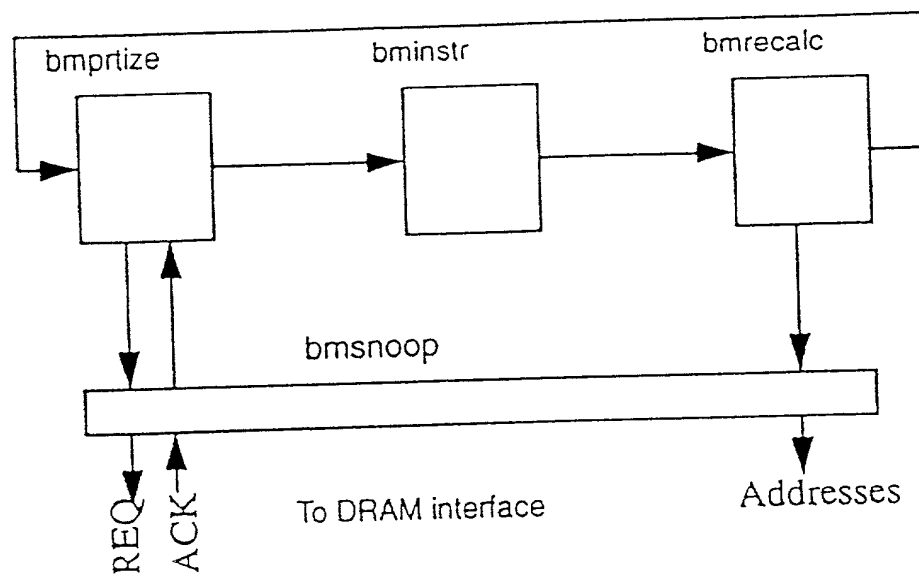


FIG. 127

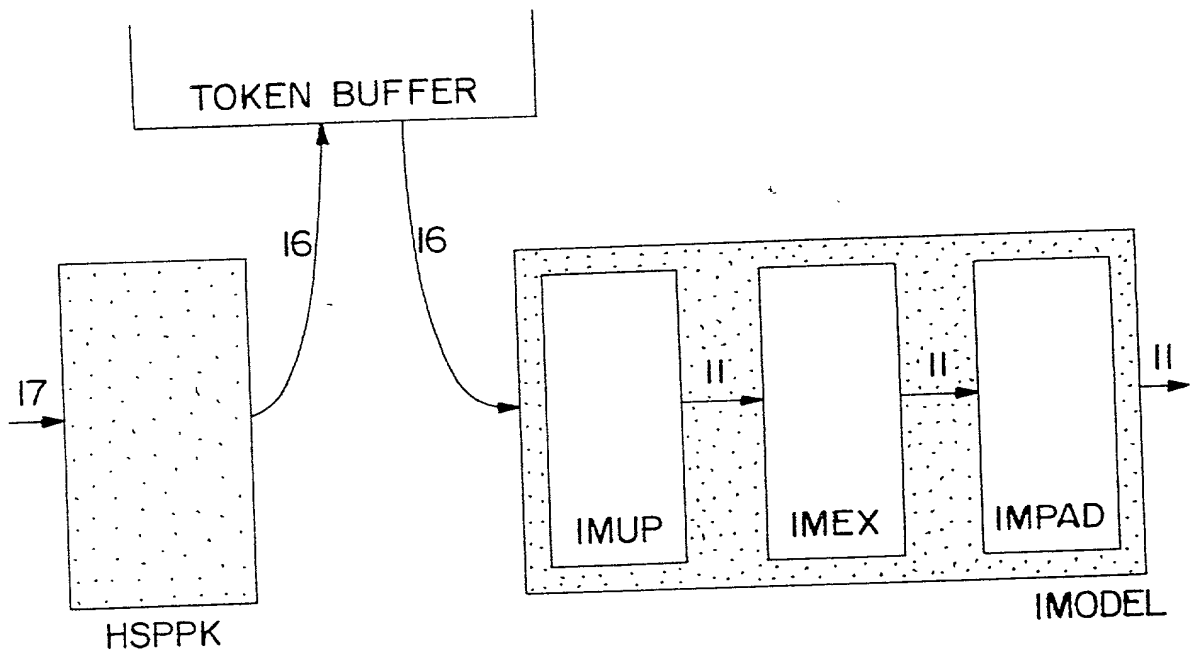


FIG. 128

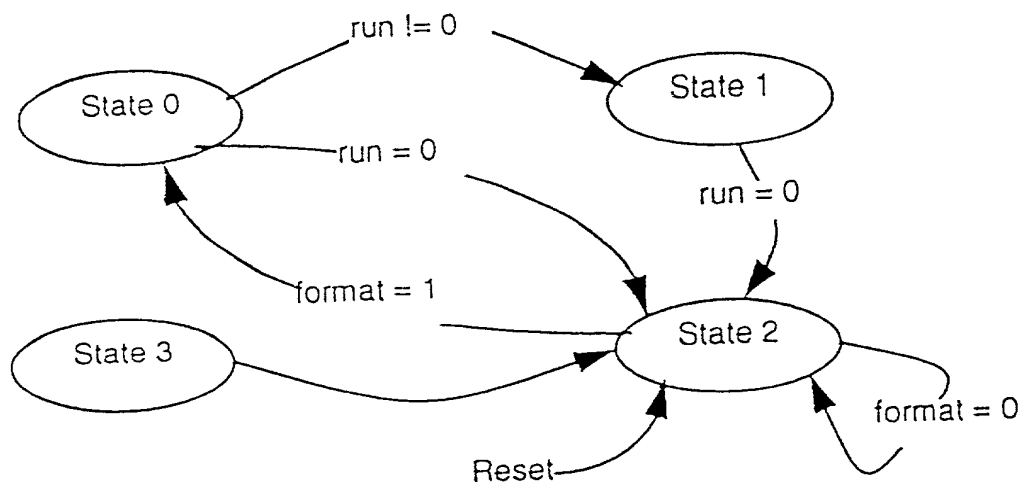


FIG. 129

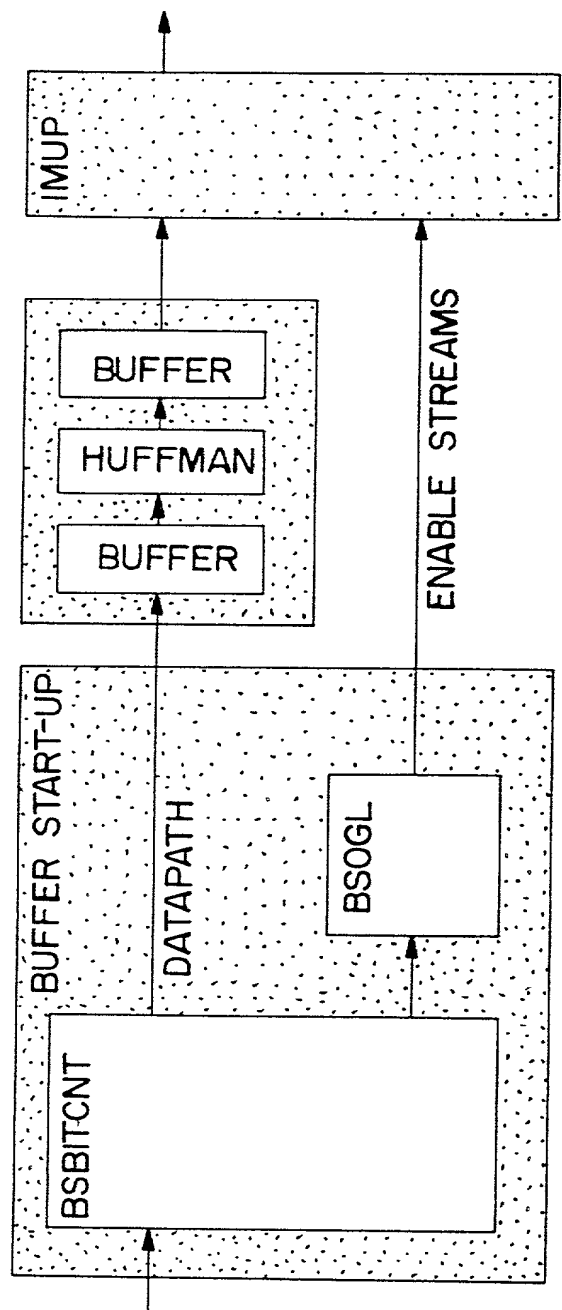


FIG. 130

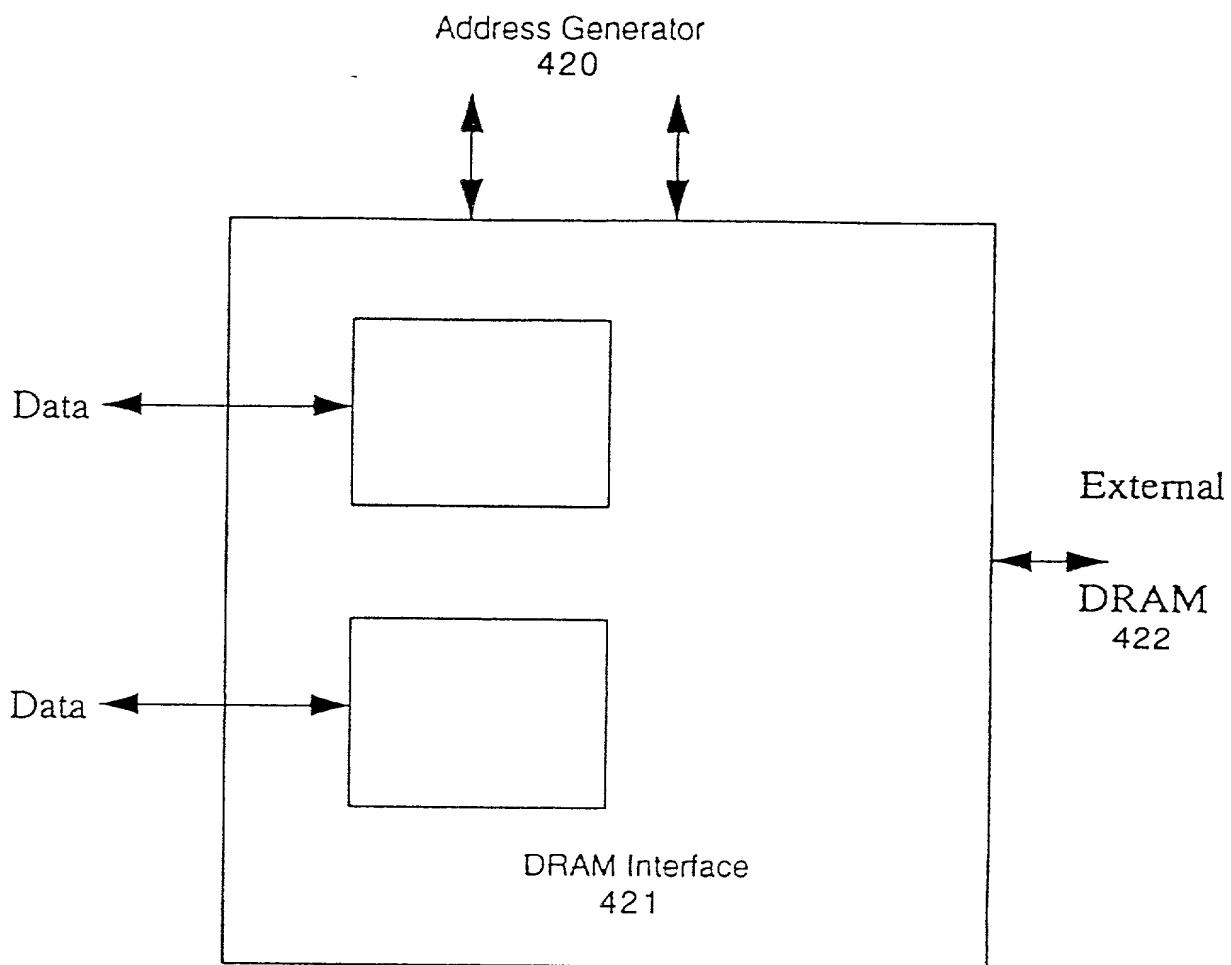


FIG. 131

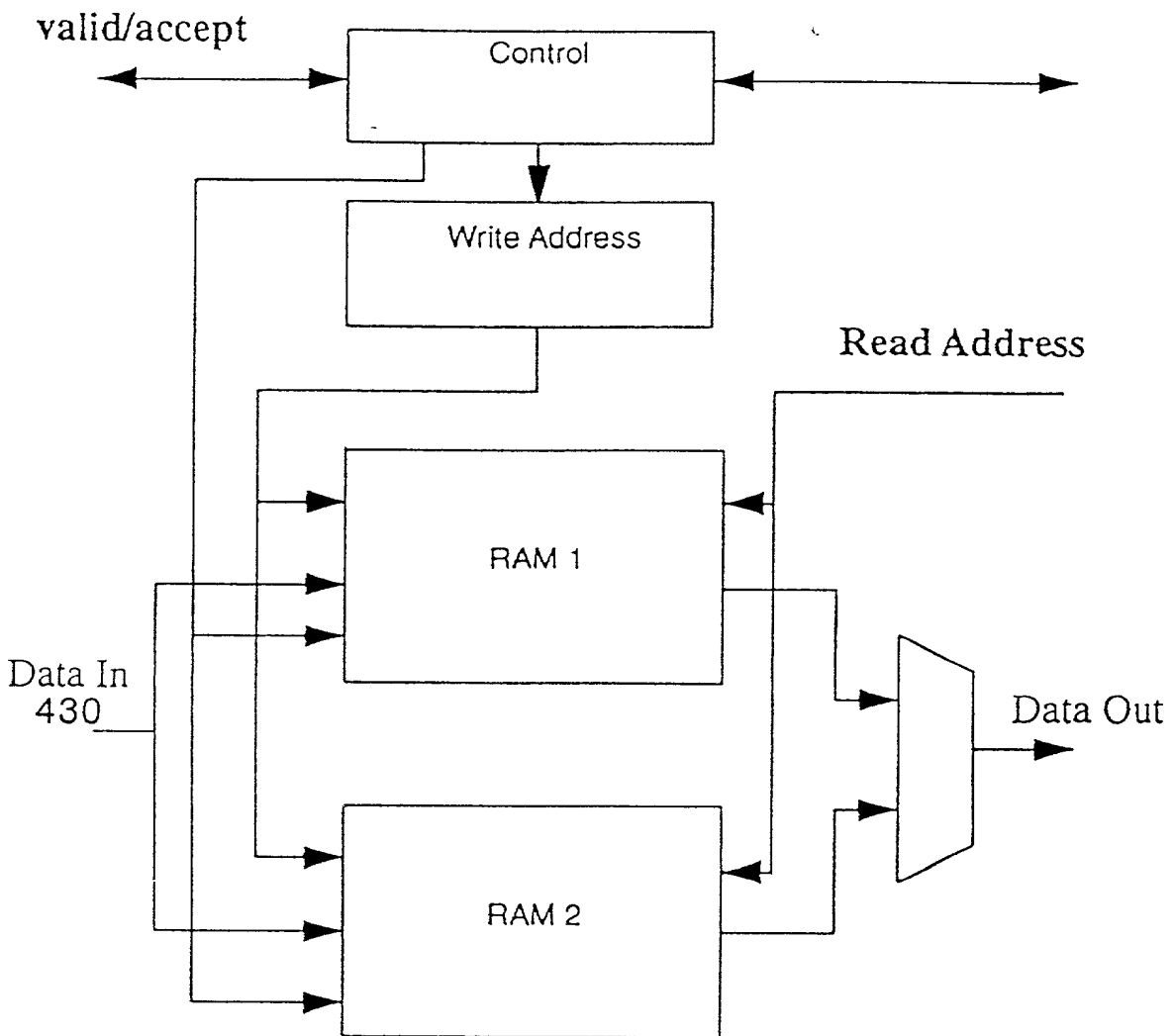


FIG. 132

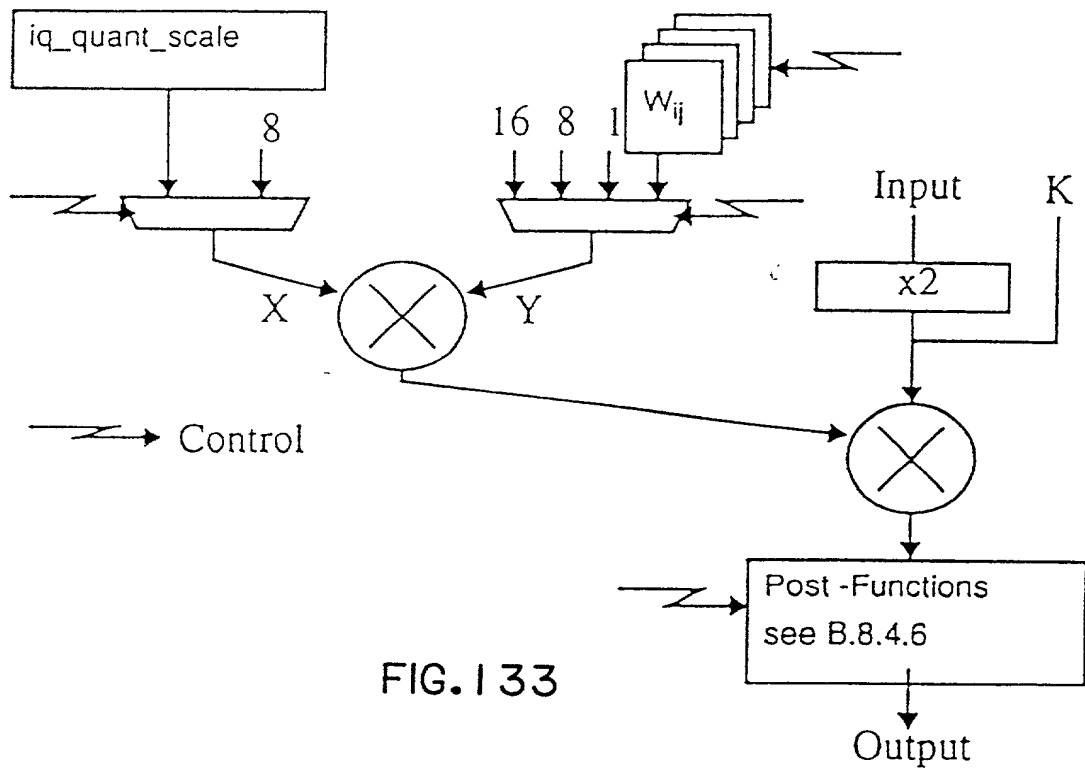


FIG. 133

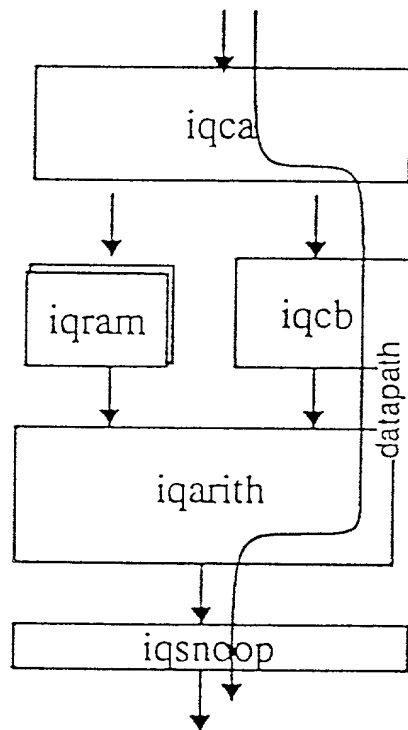


FIG. 134

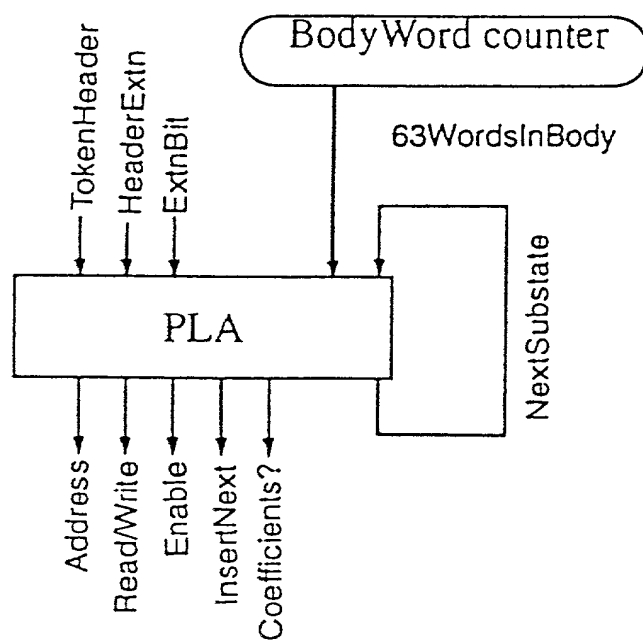


FIG. 135

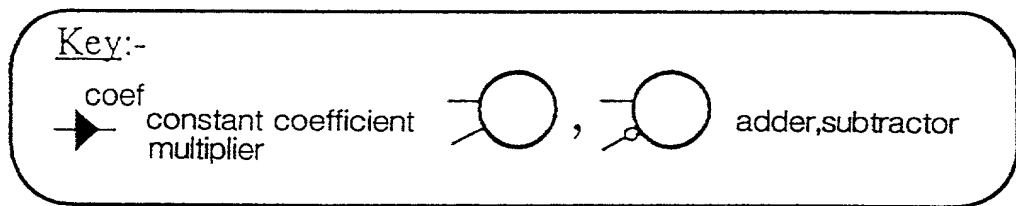
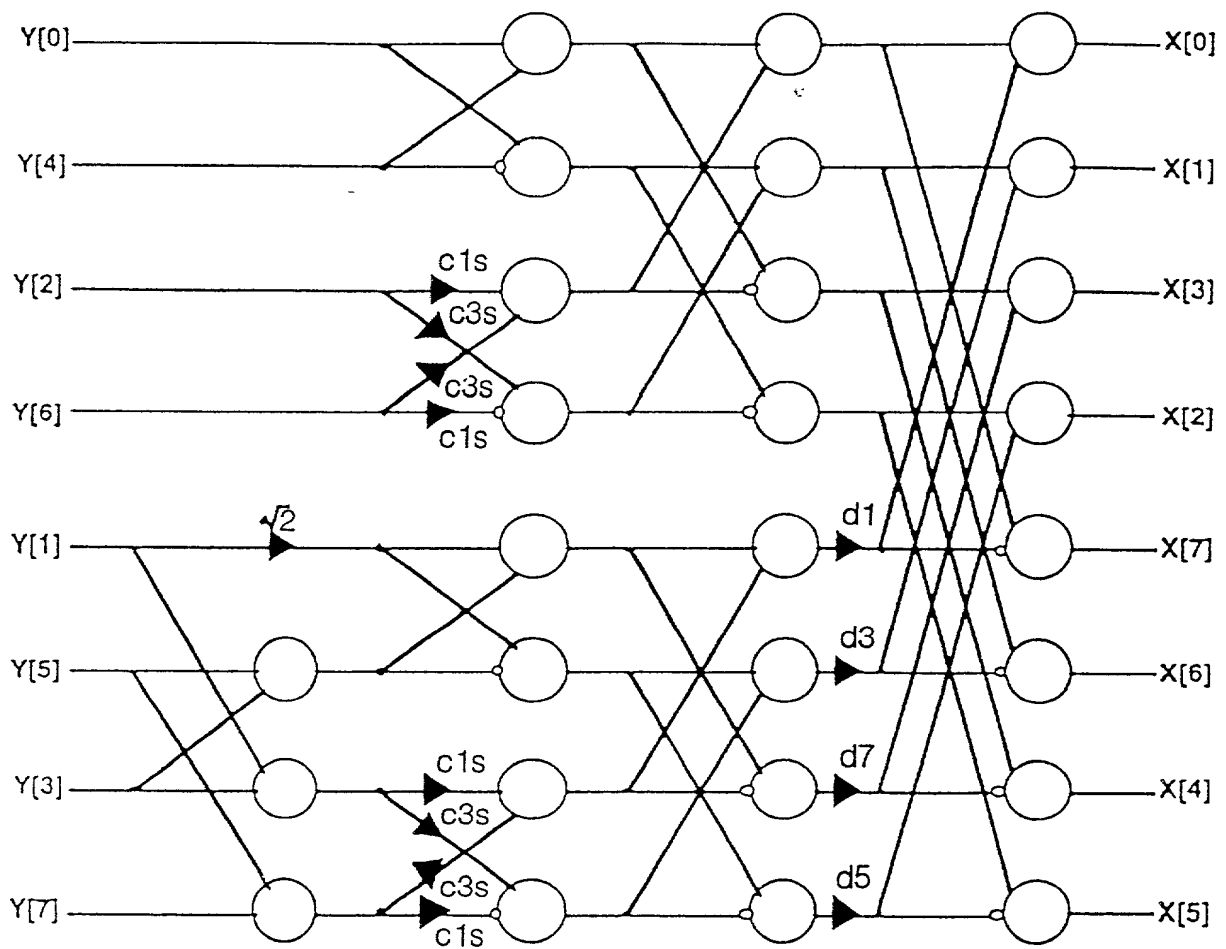


FIG. 136

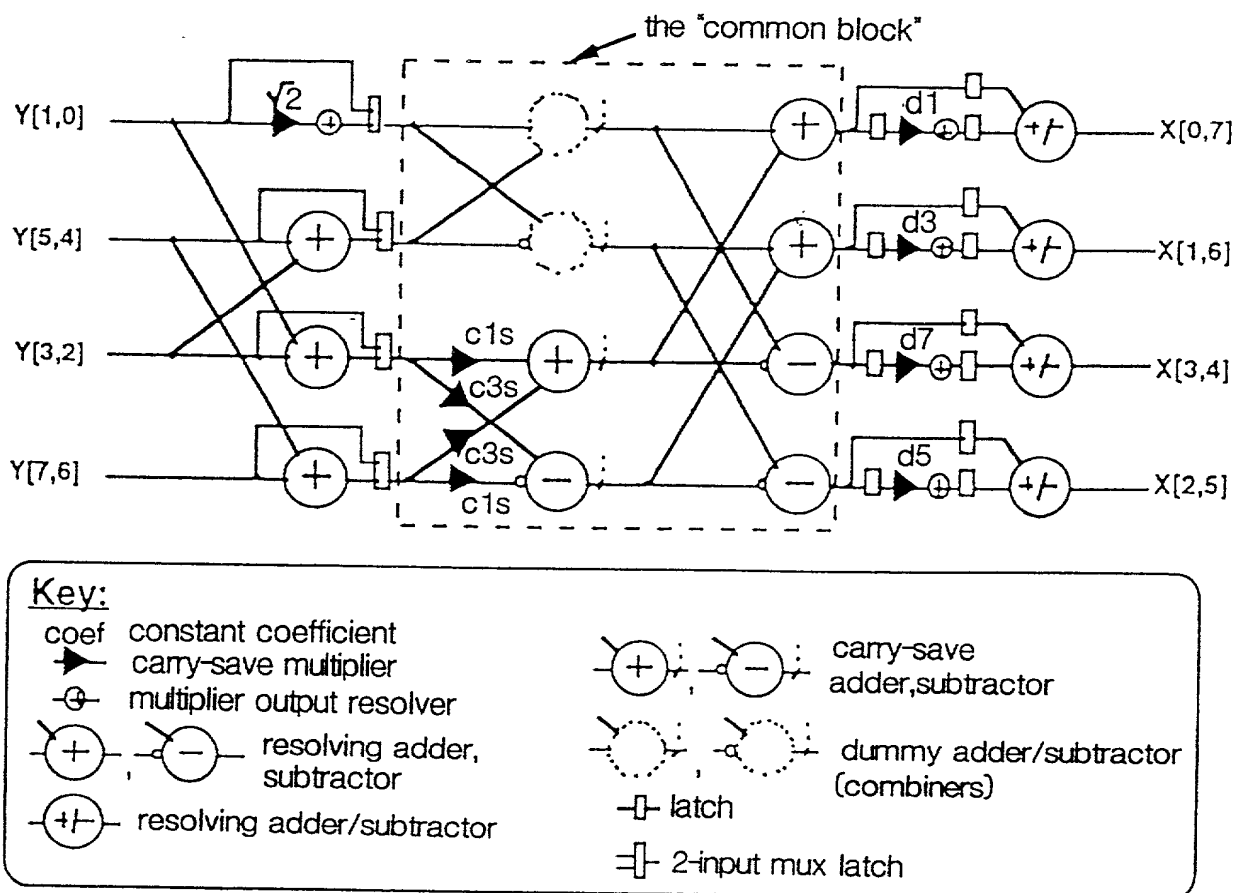


FIG. 137

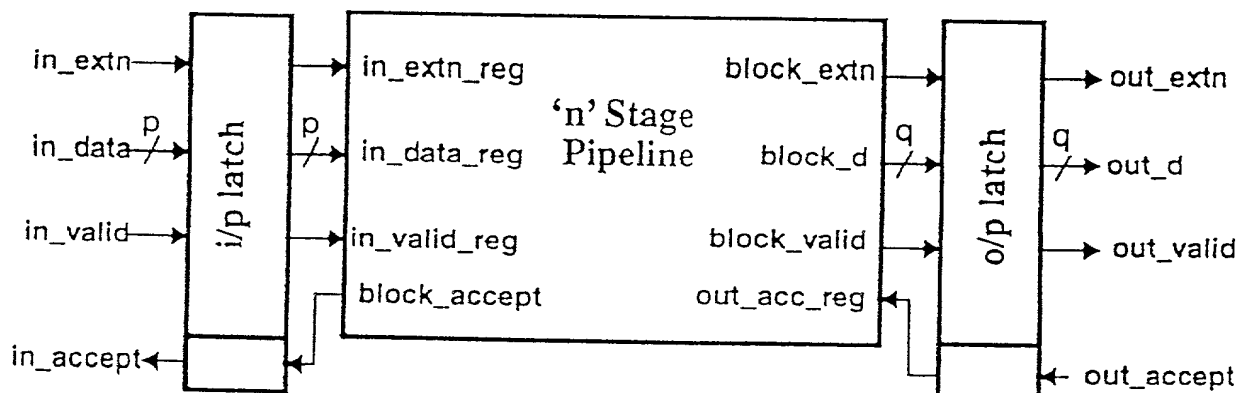


FIG. 138

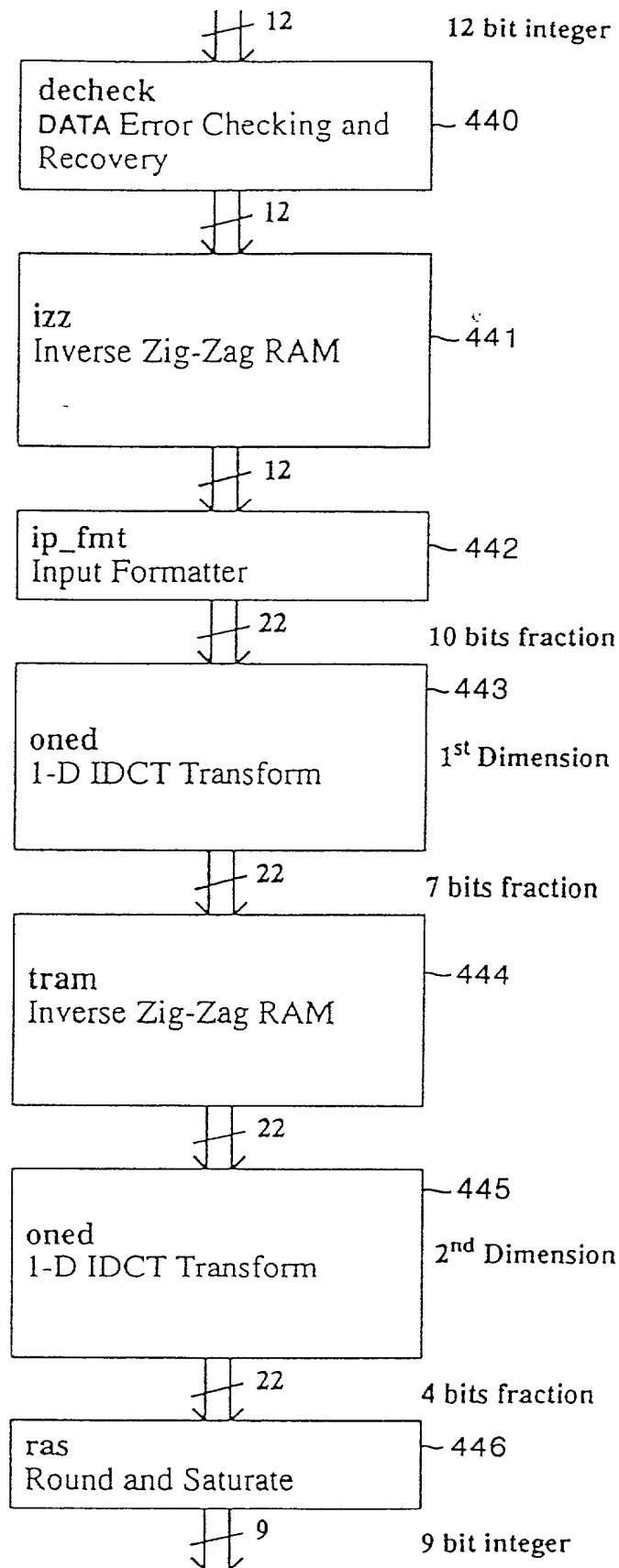


FIG. 139

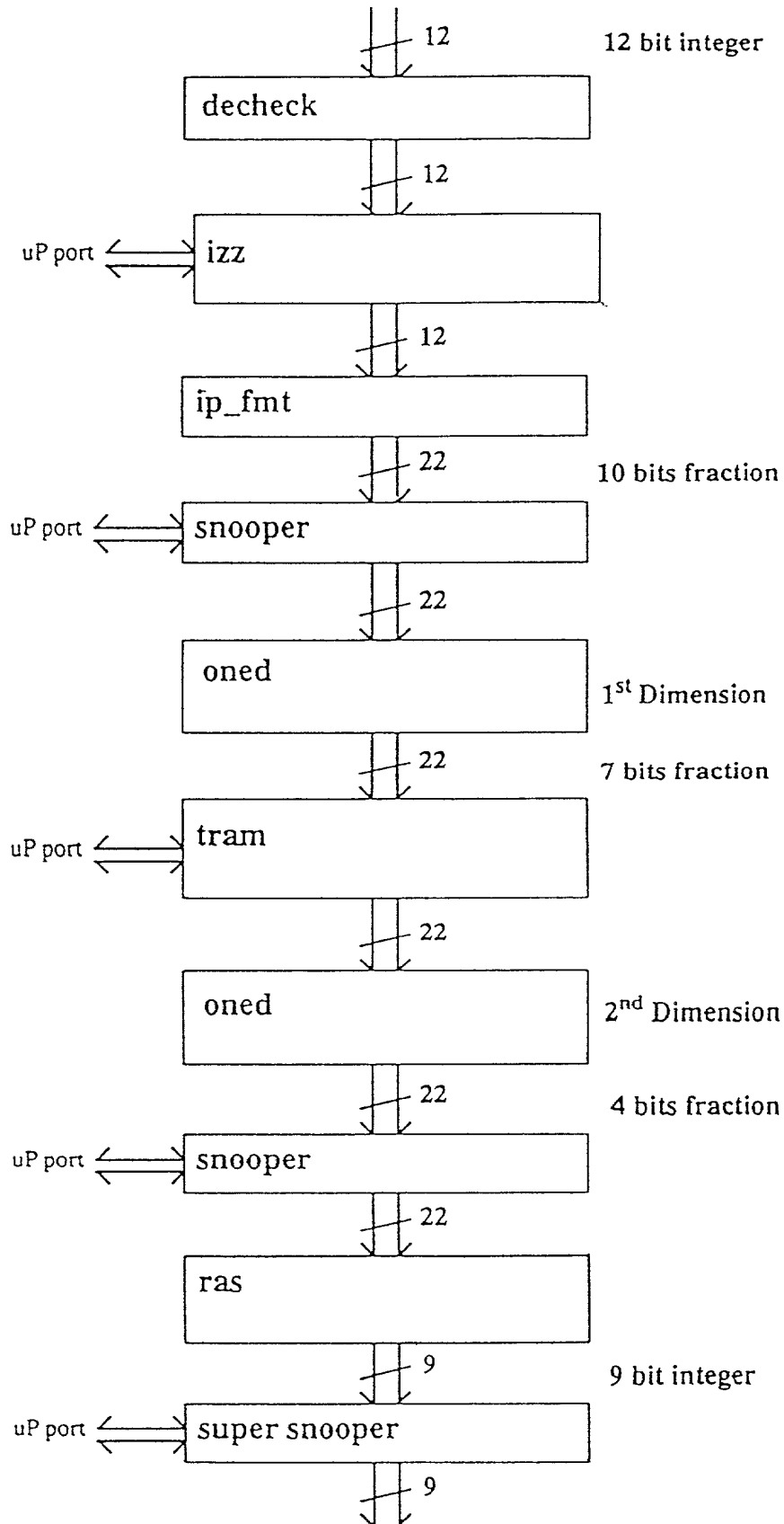


FIG. 140

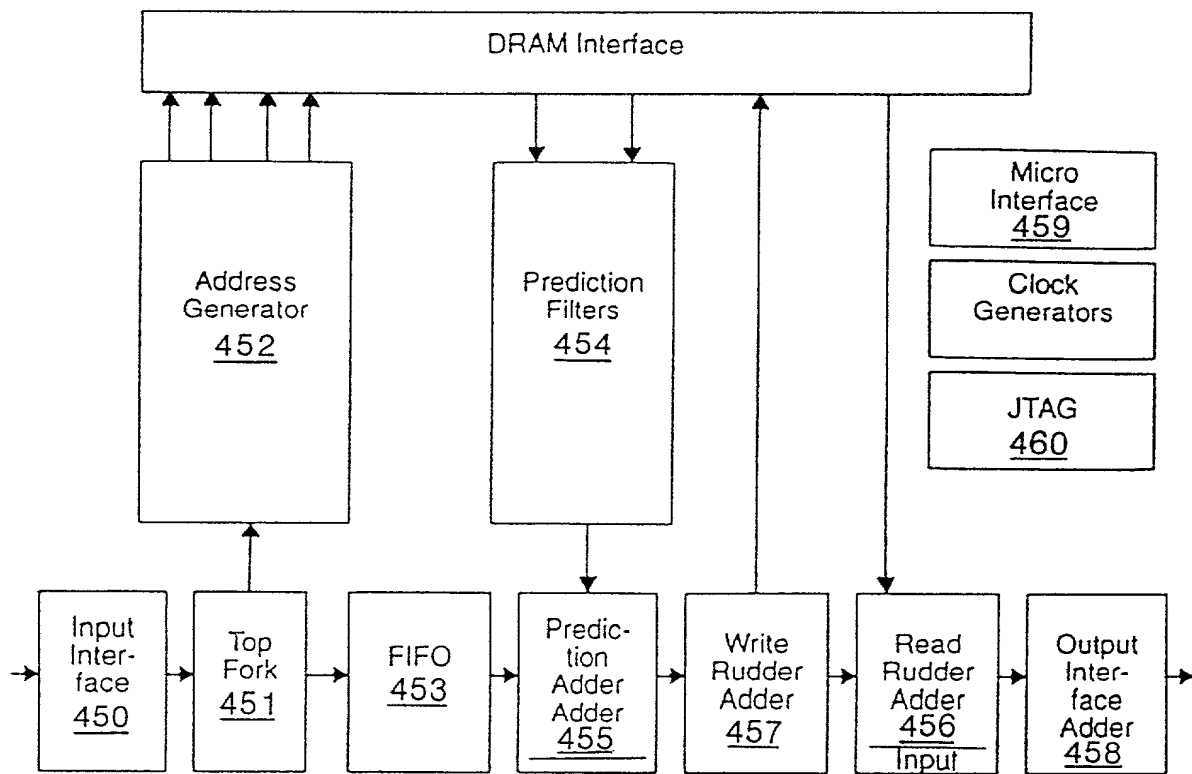


FIG. 142

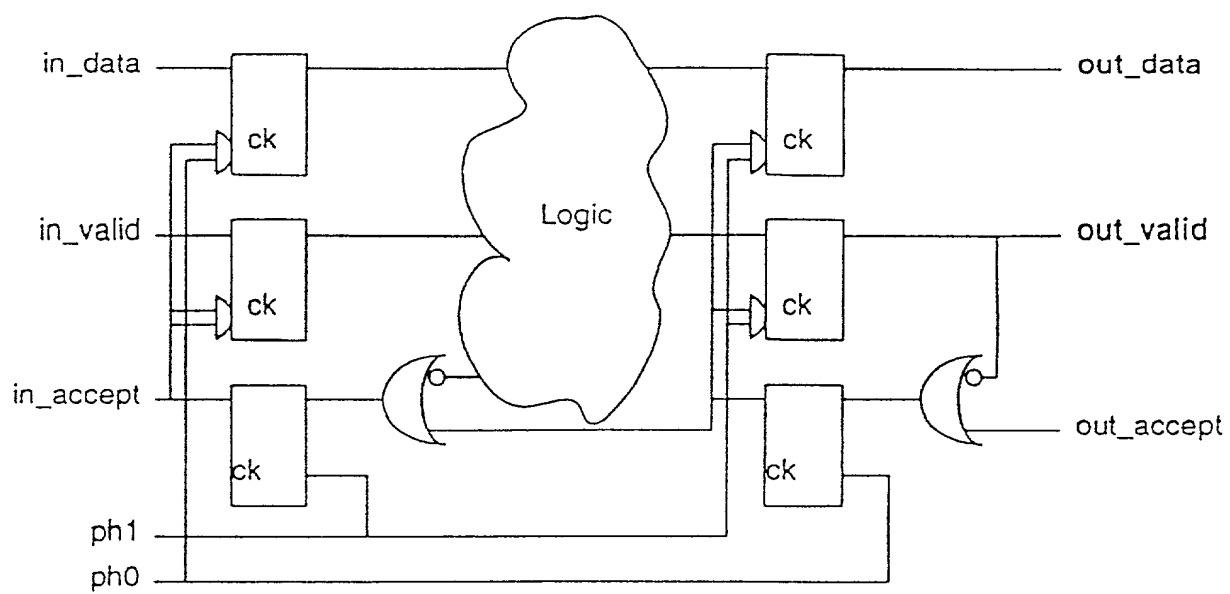


FIG. 143

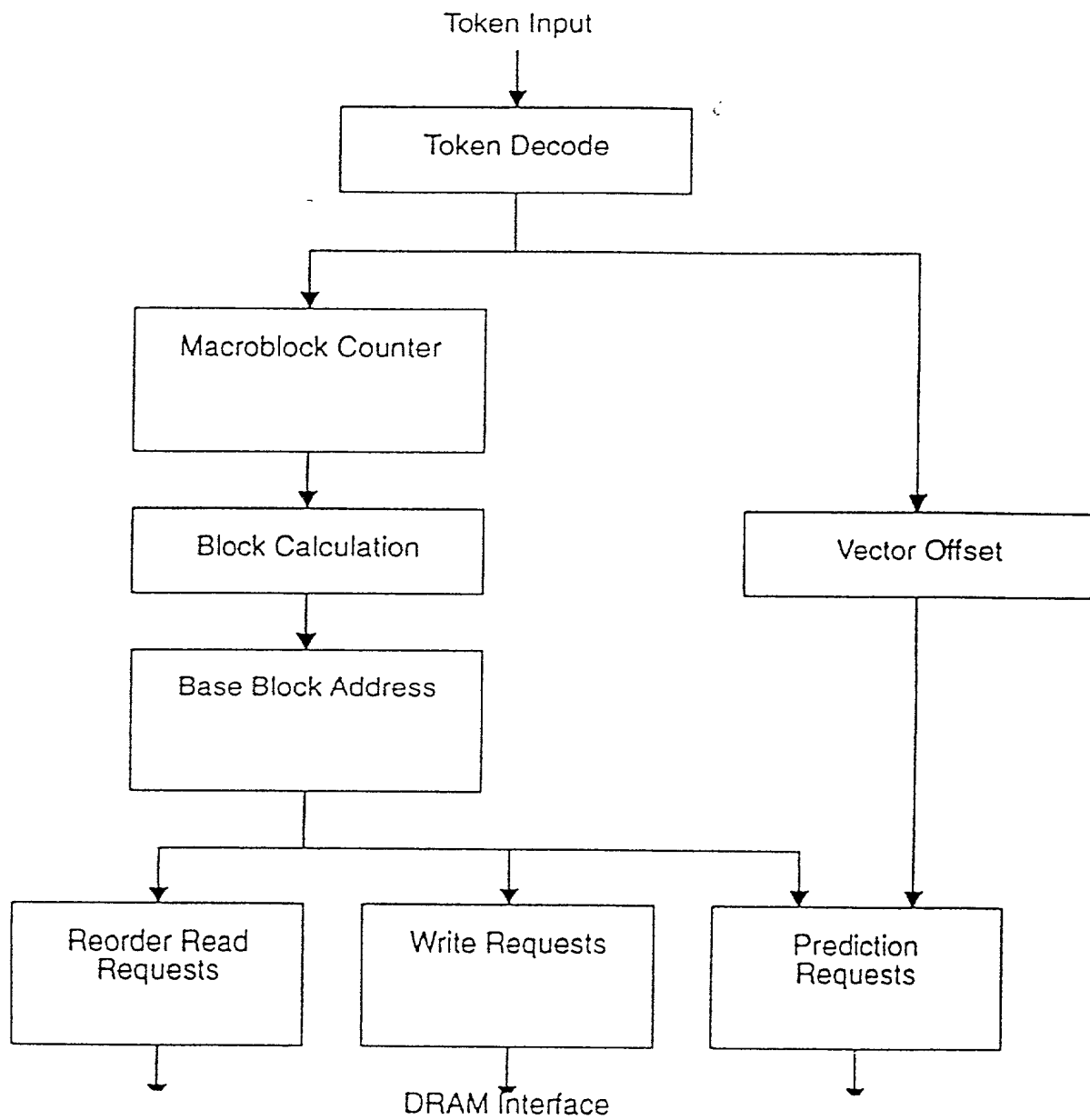


FIG. 144

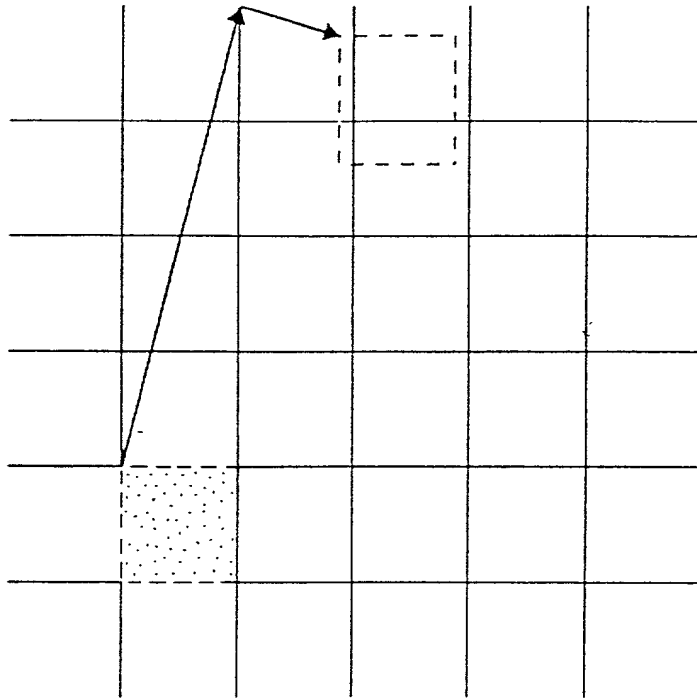


FIG. 145

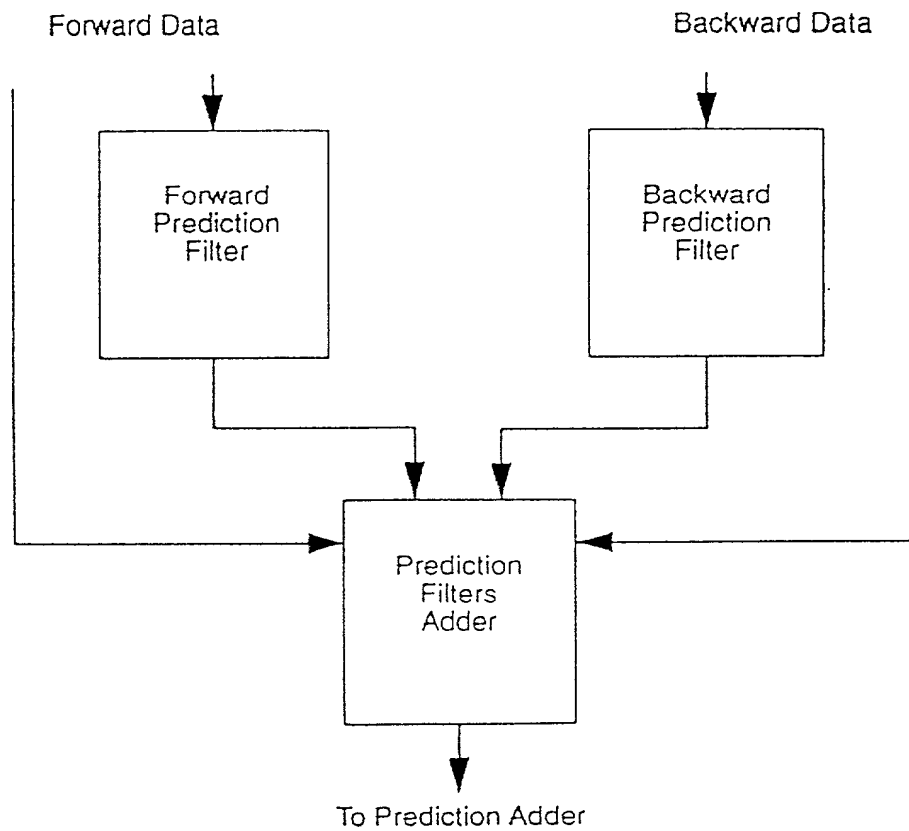


FIG. 146

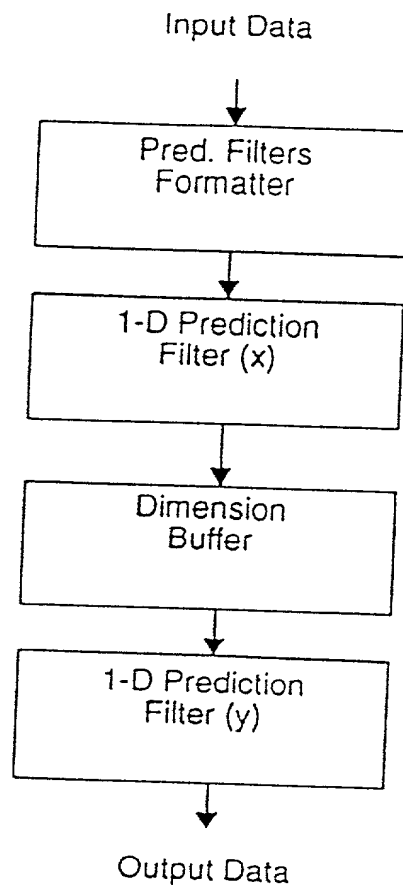


FIG. 147

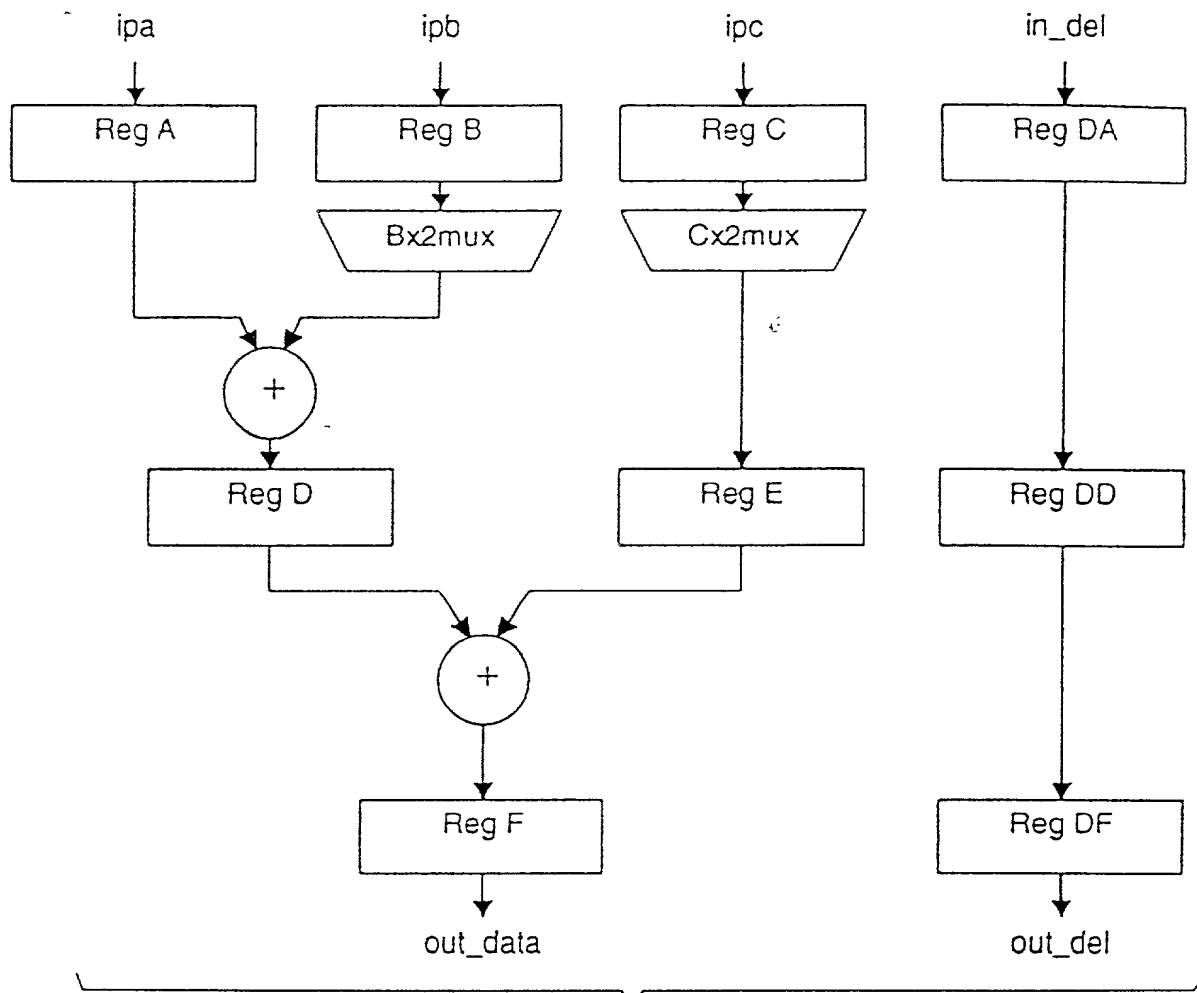


FIG. 148

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63

FIG. 149

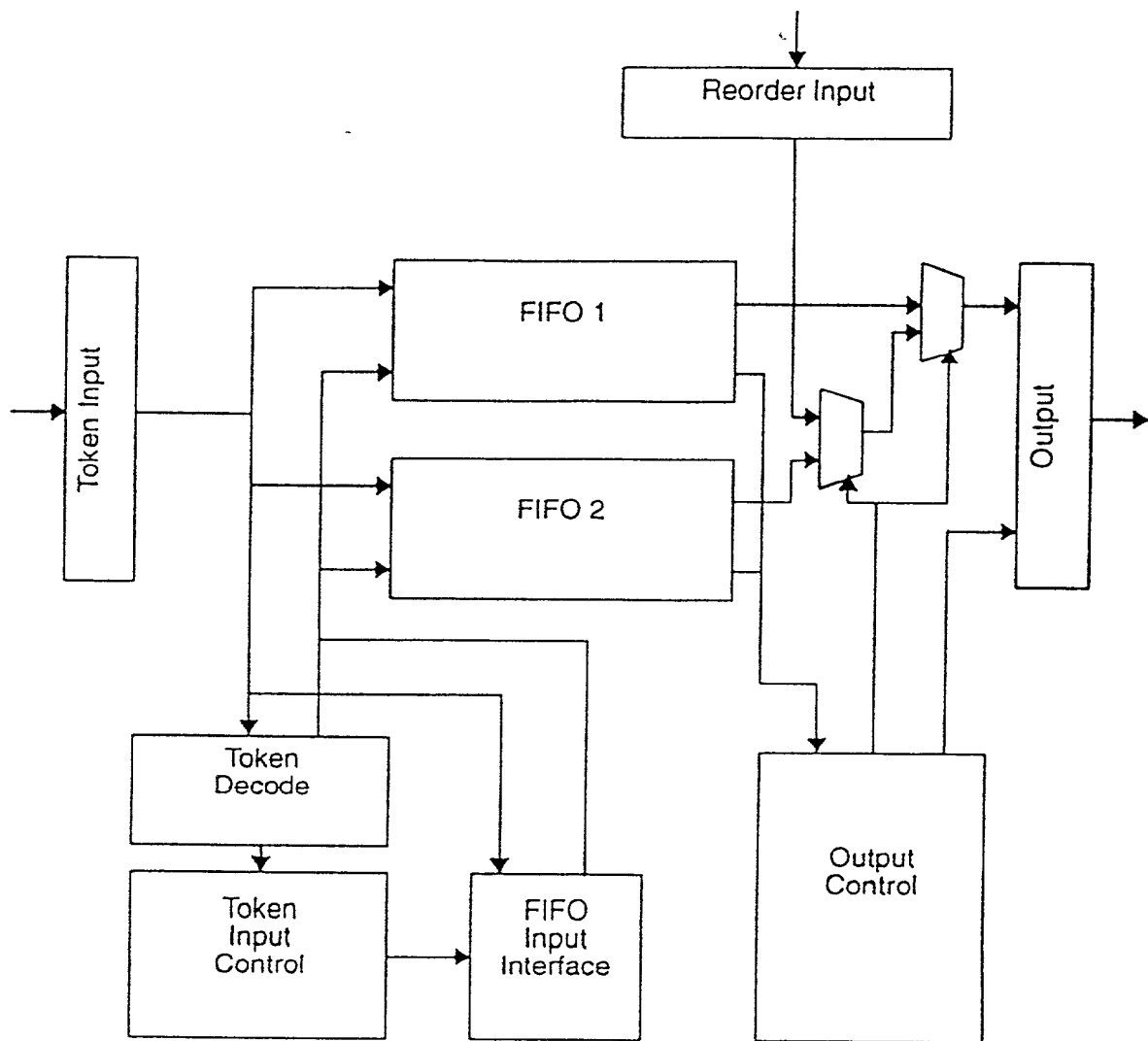


FIG. 150

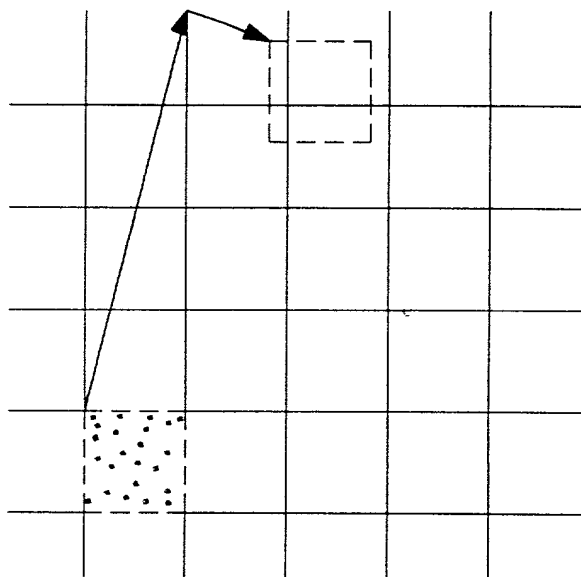


FIG. 151

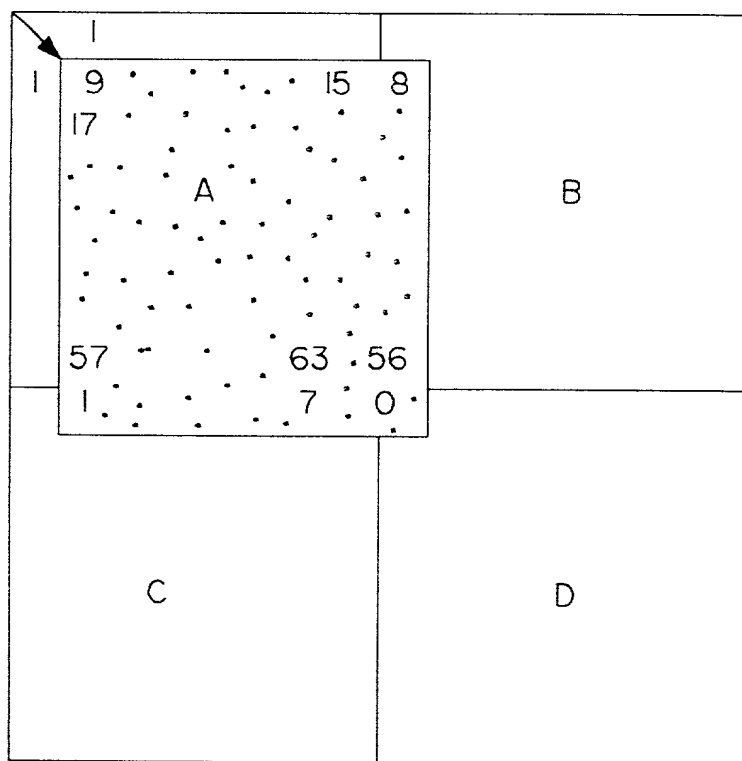


FIG. 152

Read Cycle

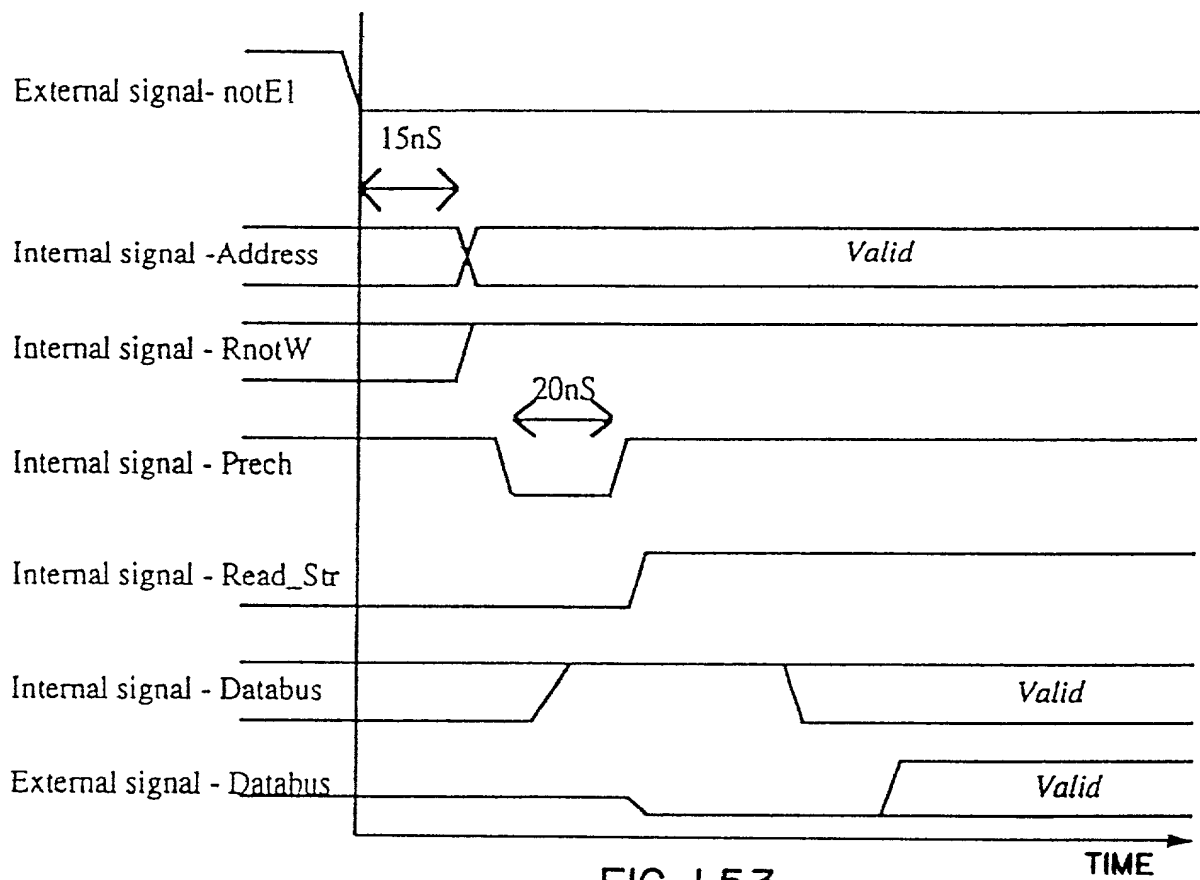
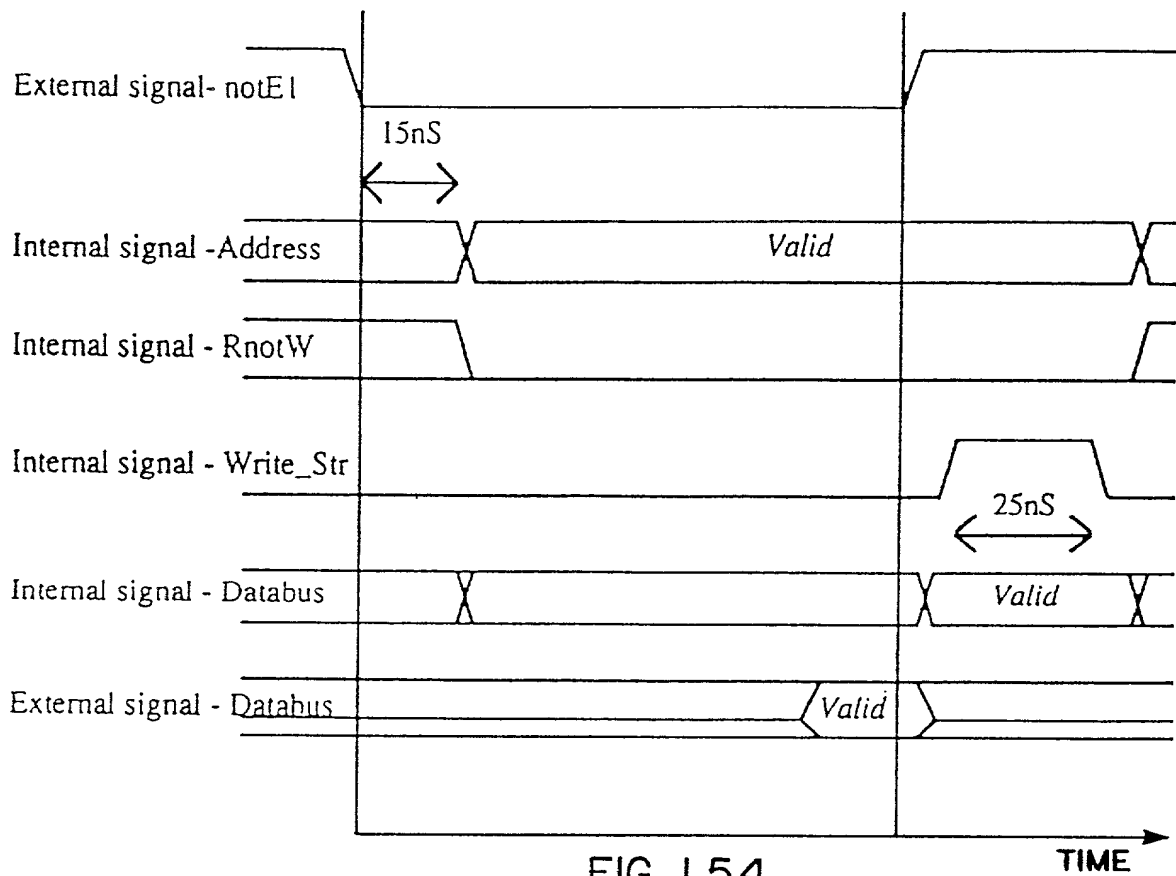


FIG. I 53

Write Cycle



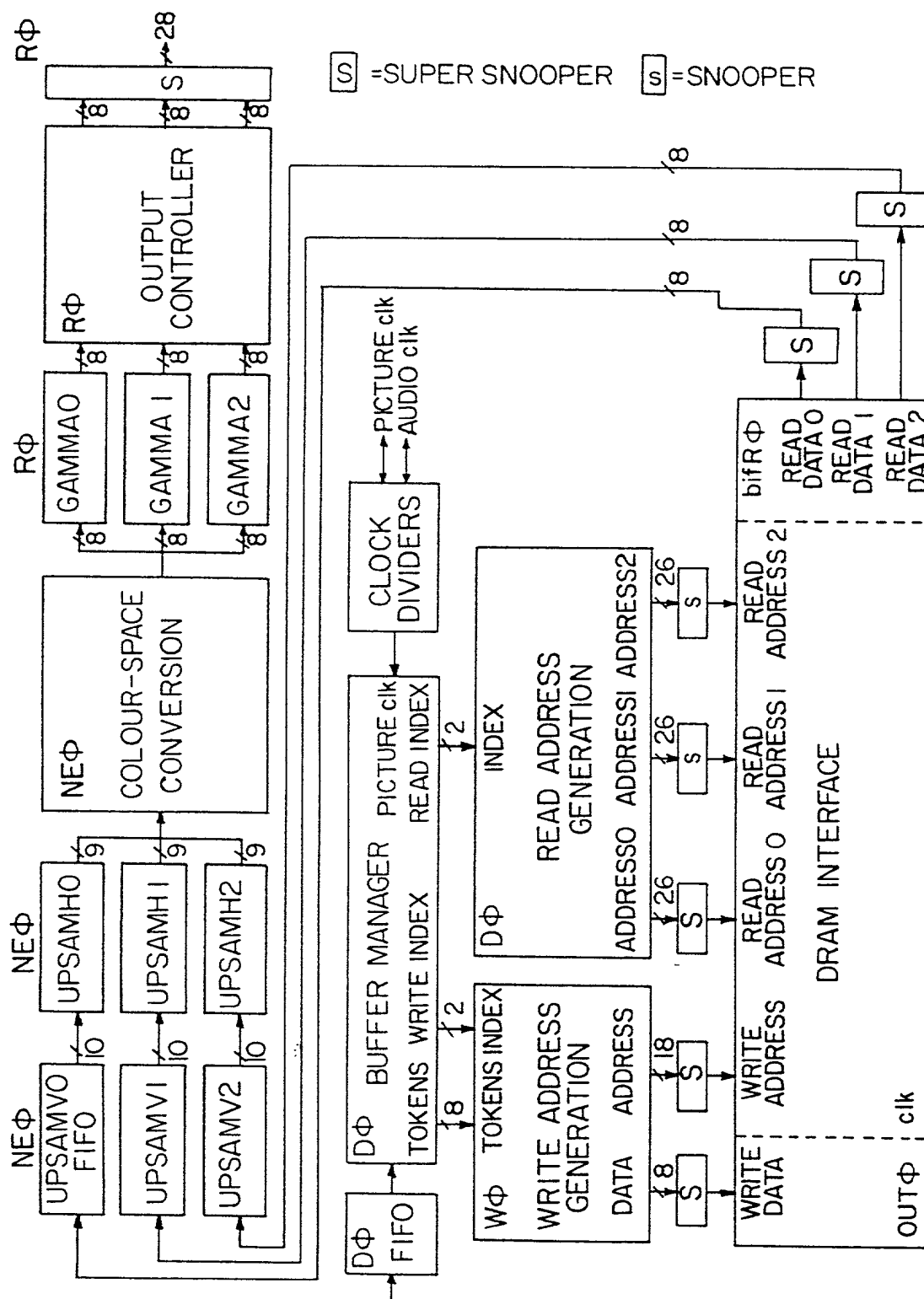


FIG. 155

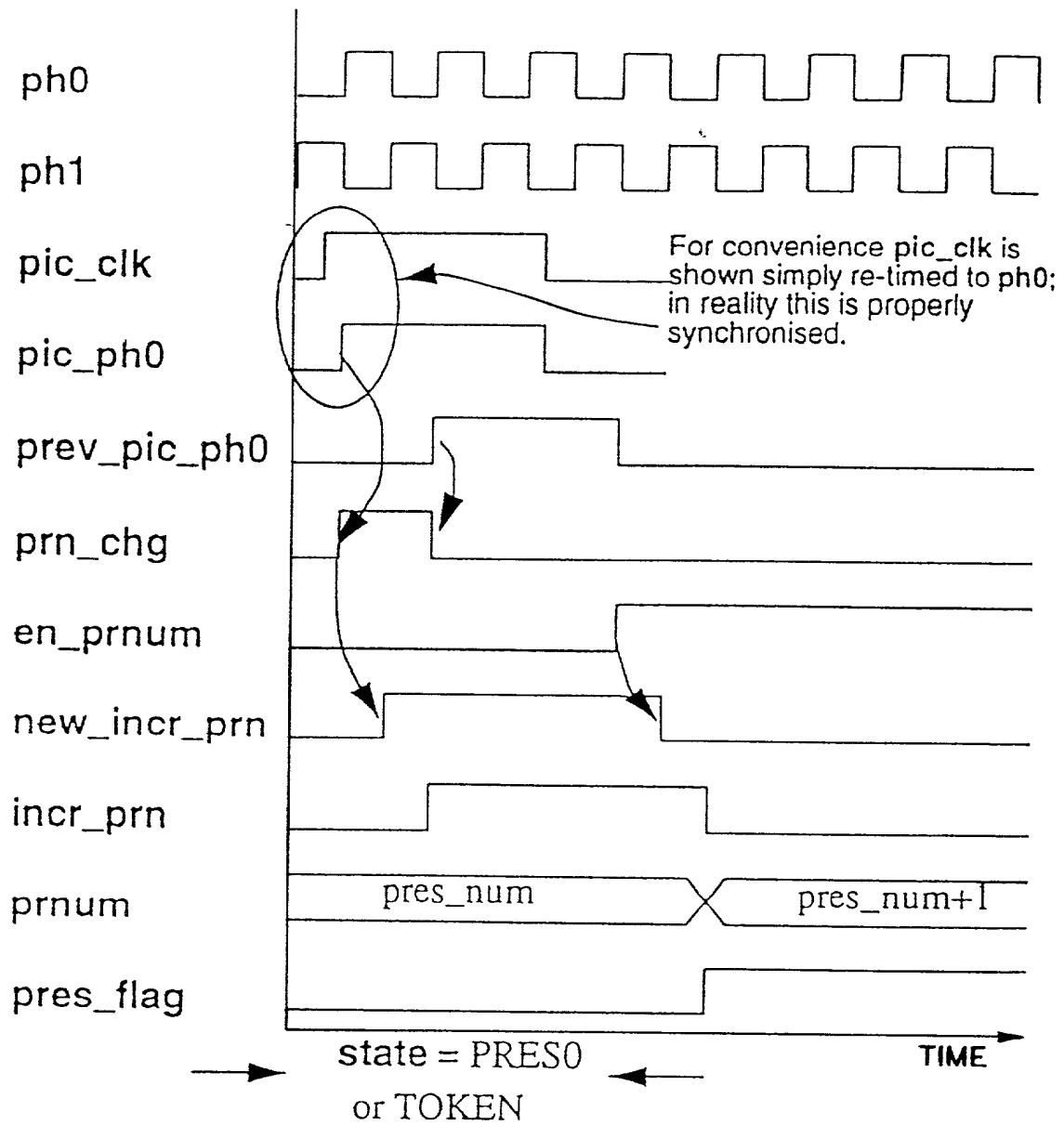
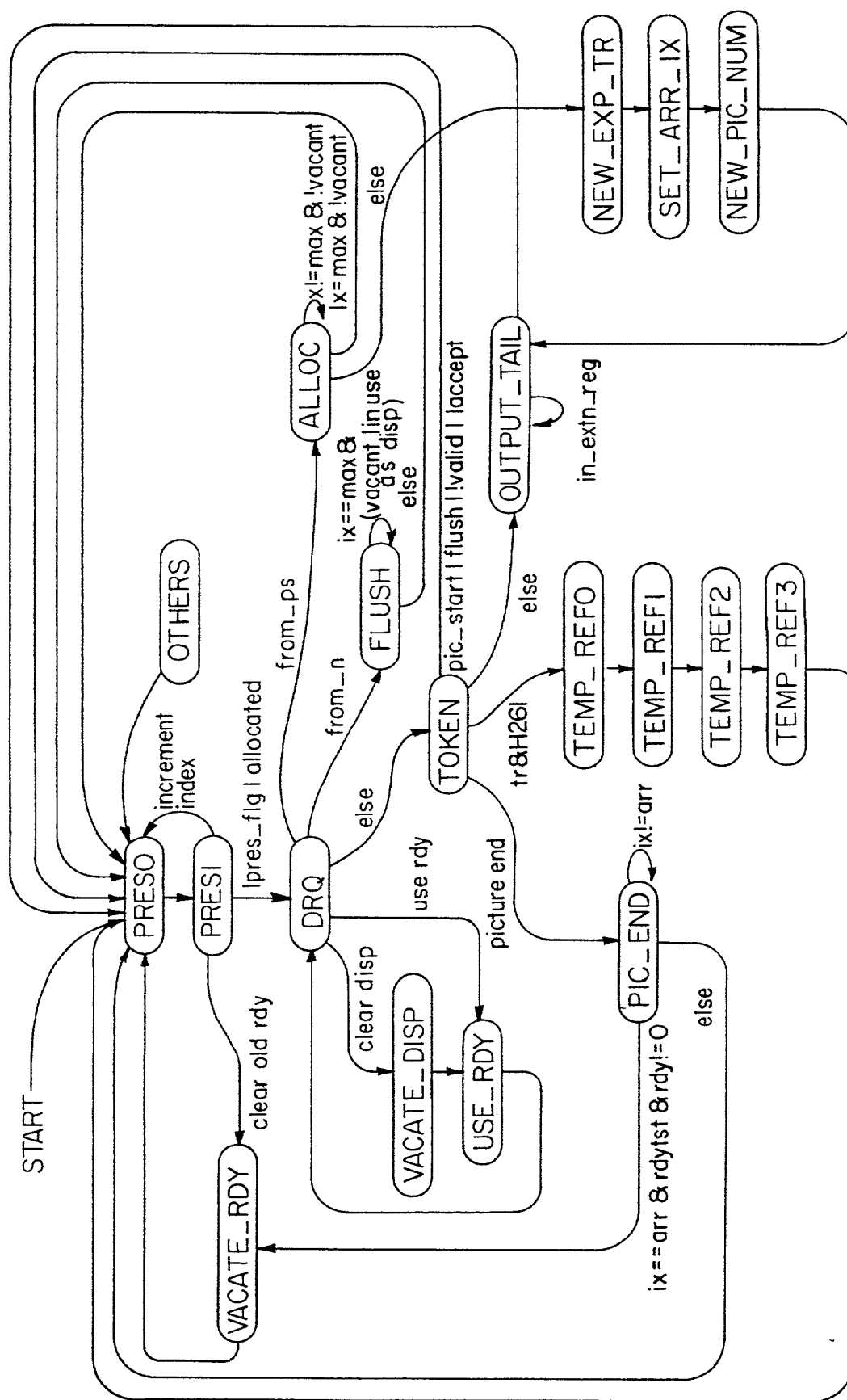


FIG. 156



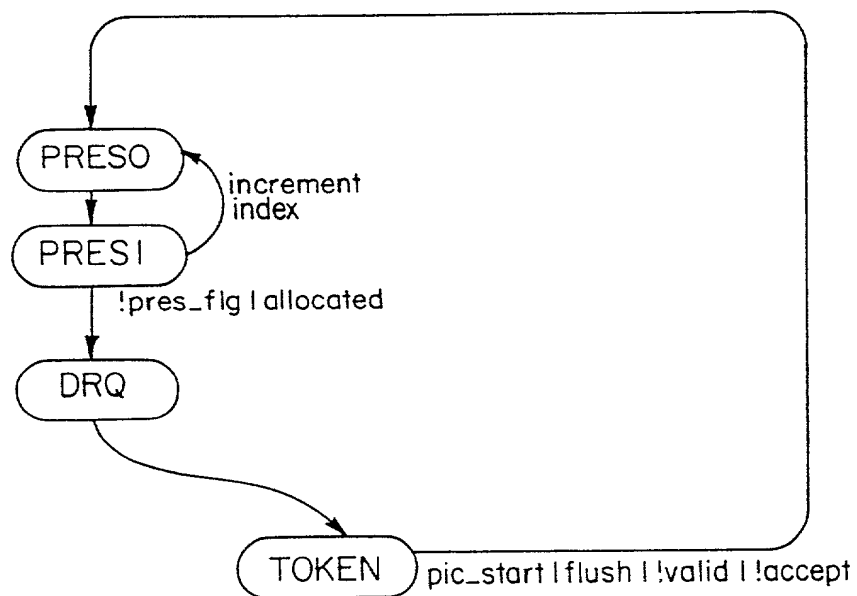


FIG. 158

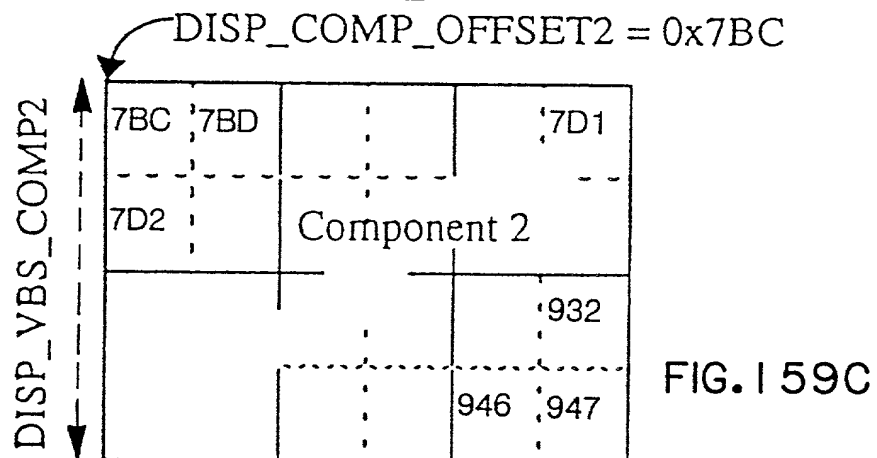
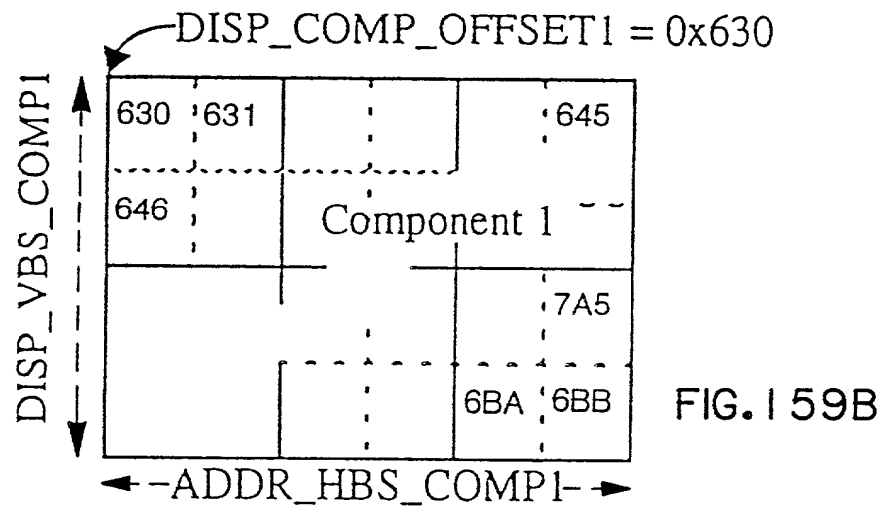
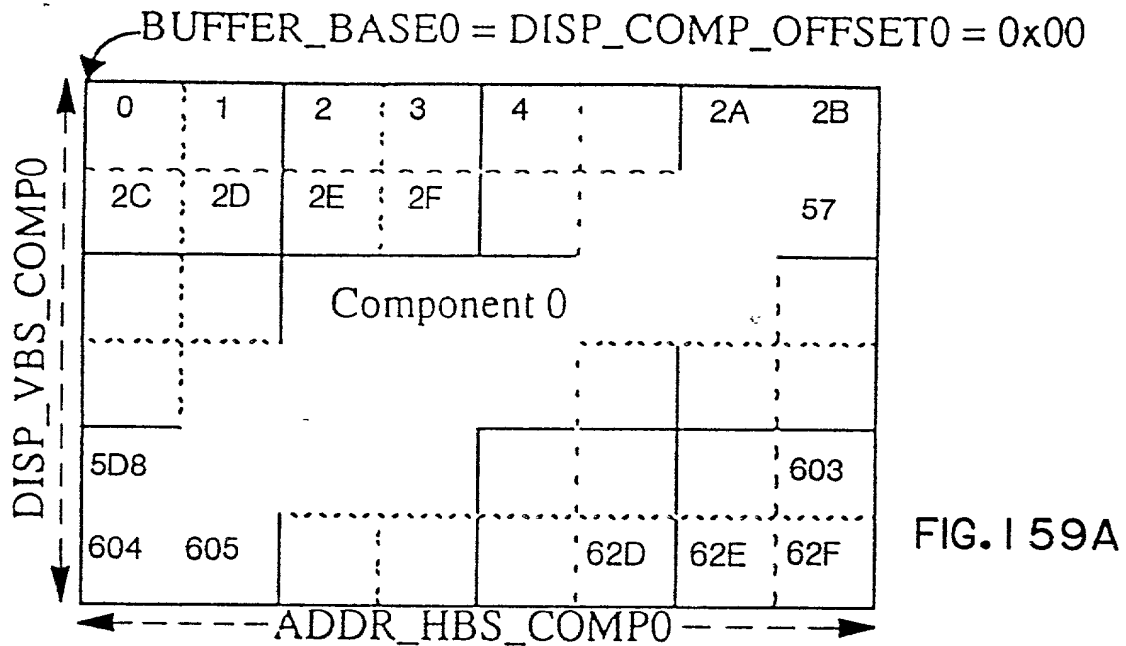


FIG. 160

BUFFER OFFSET 0x00

COMPONENT OFFSET 0x000 +

00	01	02	03	04	05	06	07	08	09	0A	0B
0C	0D	0E	0F	10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	1E	1F	20	21	22	23
24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37	38	39	3A	3B
3C	3D	3E	3F	40	41	42	43	44	45	46	47
48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
60	61	62	63	64	65	66	67	68	69	6A	6B
6C	6D	6E	6F	70	71	72	73	74	75	76	77
78	79	7A	7B	7C	7D	7E	7F	80	81	82	83
84	85	86	87	88	89	8A	8B	8C	8D	8E	8F

FIG.161A

COMPONENT1 OFFSET 0x100 +

00	01	02	03	04	05
06	07	08	09	0A	0B
0C	0D	0E	0F	10	11
12	13	14	15	16	17
18	19	1A	1B	1C	1D
1E	1F	20	21	22	23

FIG.161B

COMPONENT1 OFFSET 0x200 +

00	01	02	03	04	05
06	07	08	09	0A	0B
0C	0D	0E	0F	10	11
12	13	14	15	16	17
18	19	1A	1B	1C	1D
1E	1F	20	21	22	23

FIG.161C

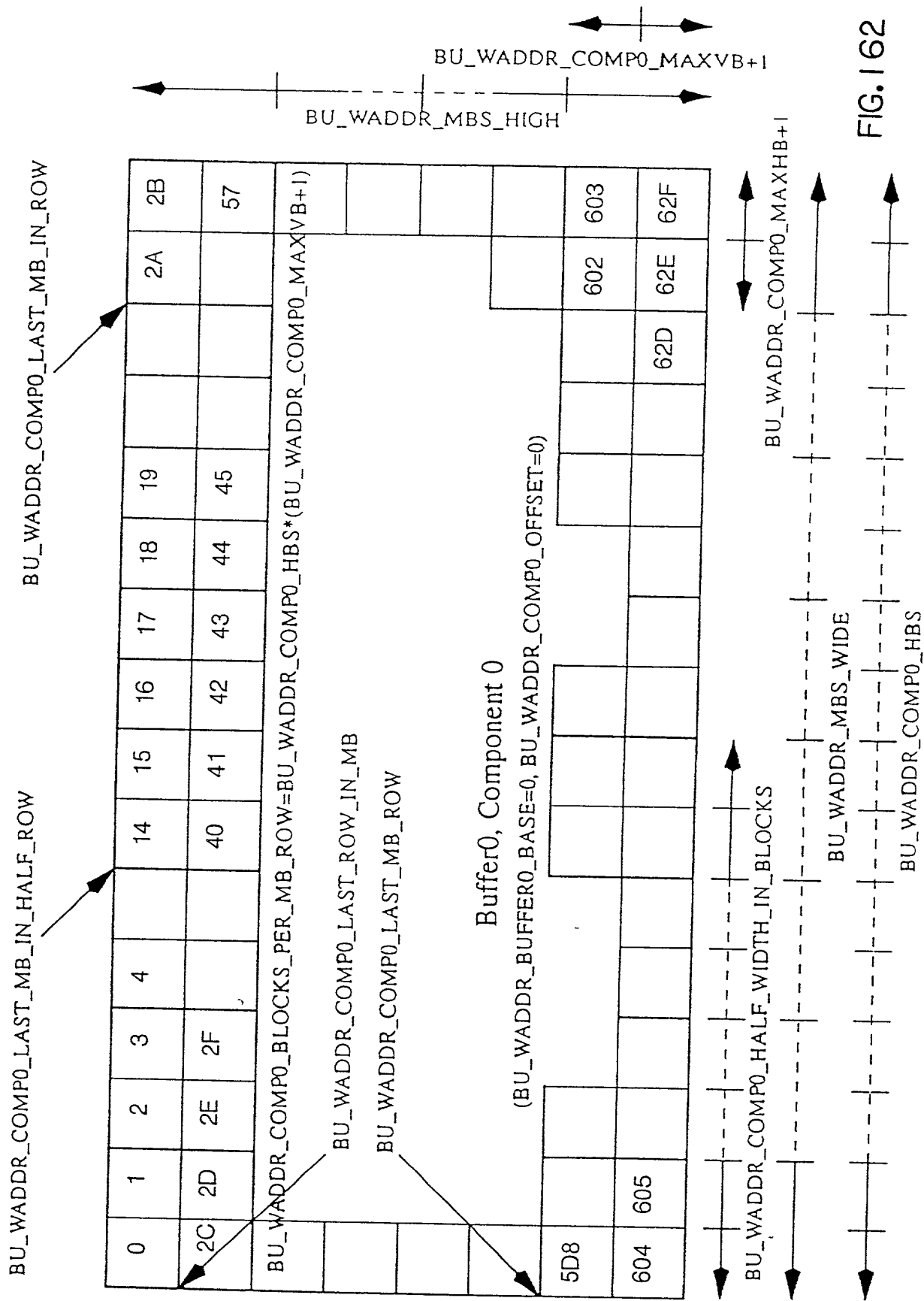
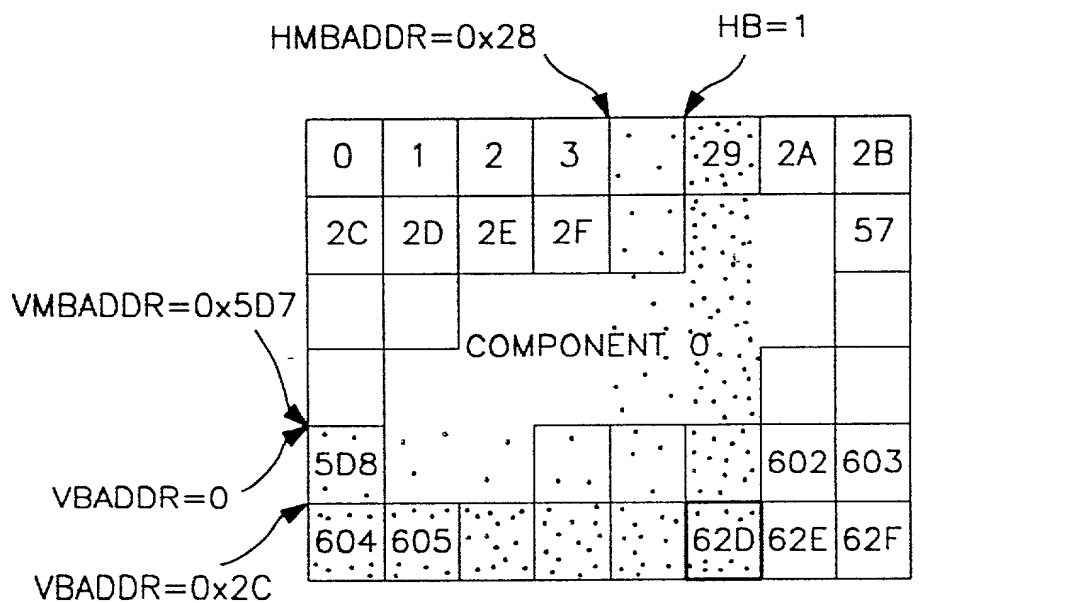
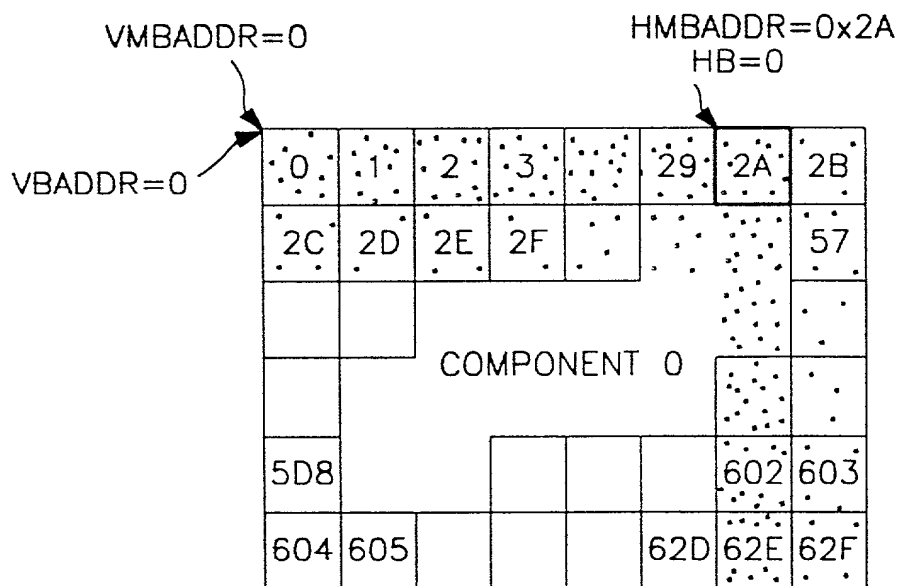


FIG. 162



$$\text{BLOCK ADDRESS} = 0 + 0 + 0 + 0x5D8 + 0x28 + 0x2C + 1 = 0x62D$$

FIG. 163A



$$\text{BLOCK ADDRESS} = 0 + 0 + 0 + 0x2A + 0 + 0 = 0x2A$$

FIG. 163B

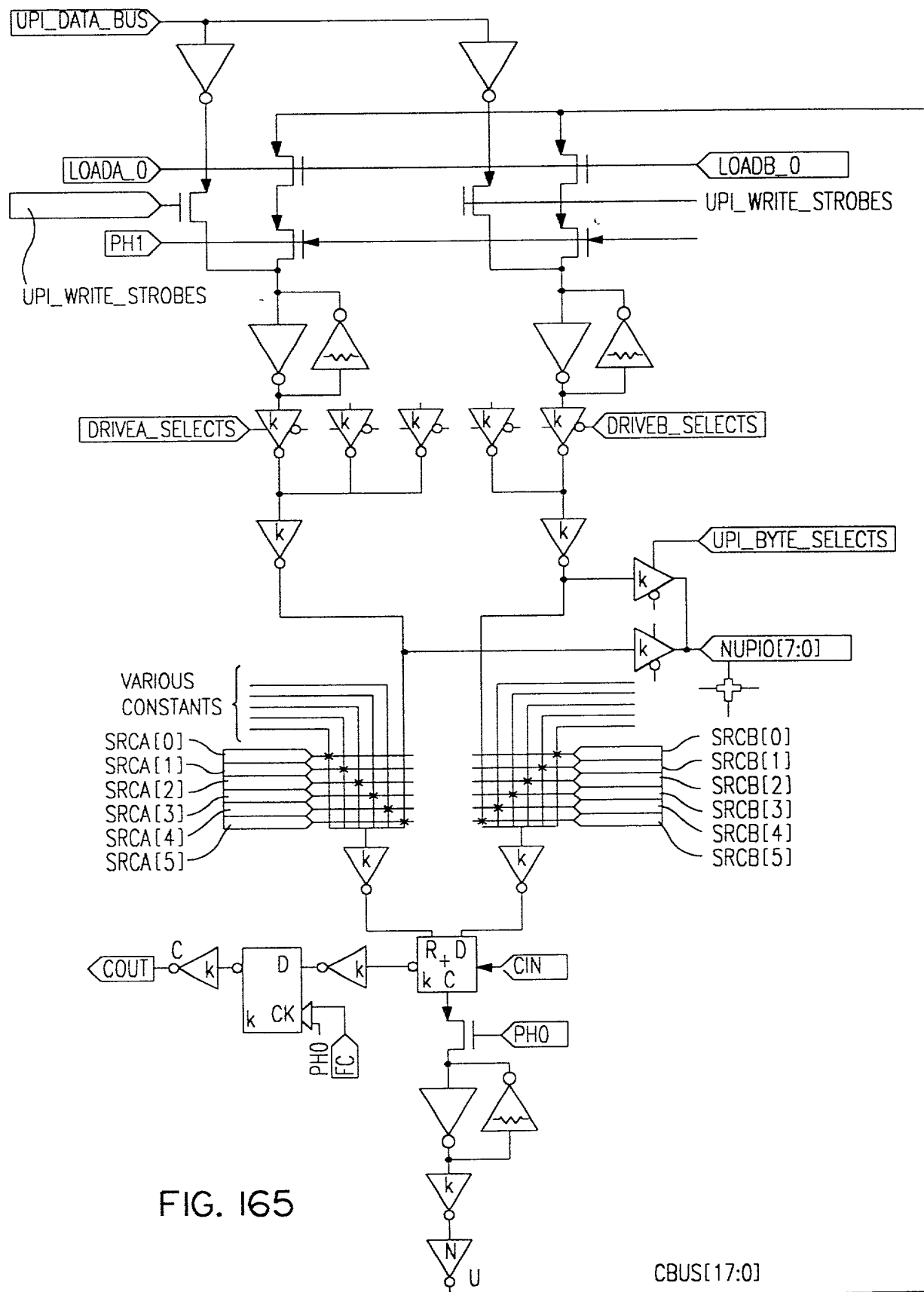


FIG. 165

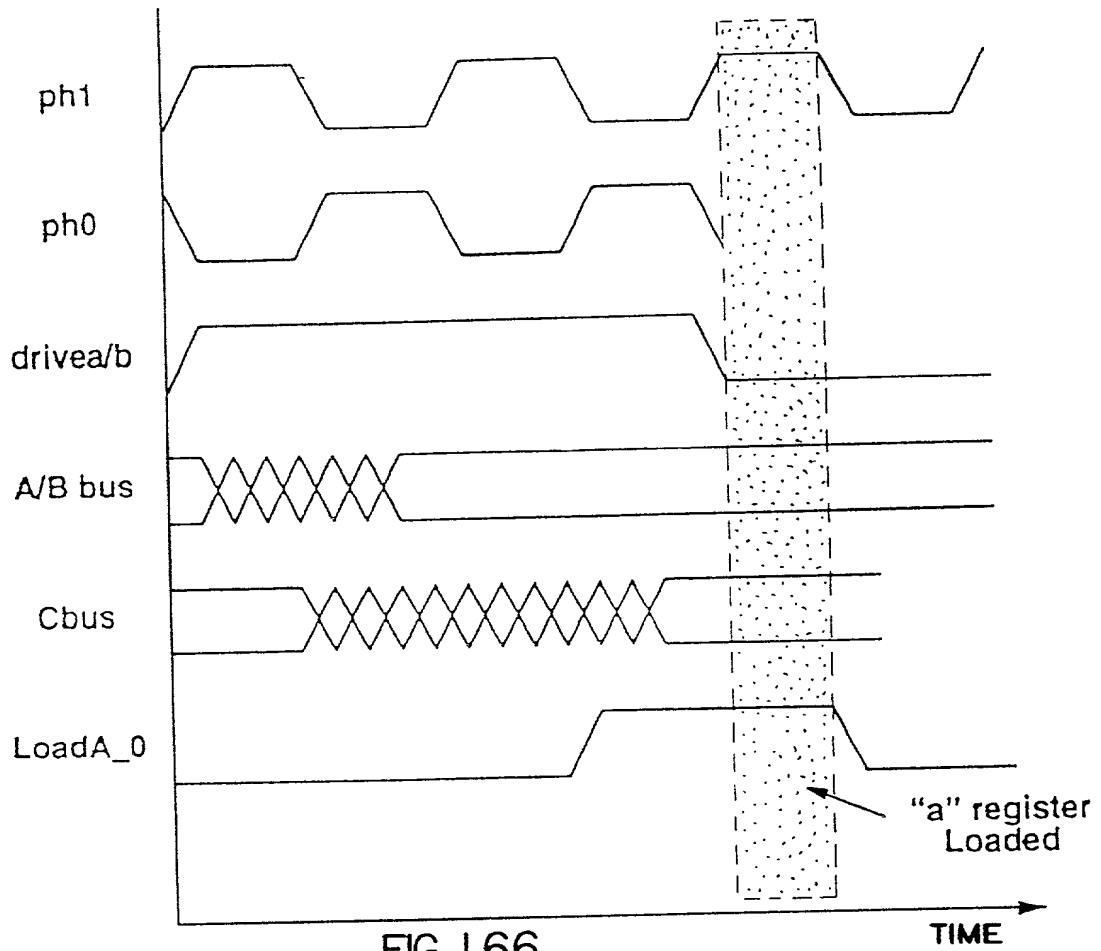


FIG. 166

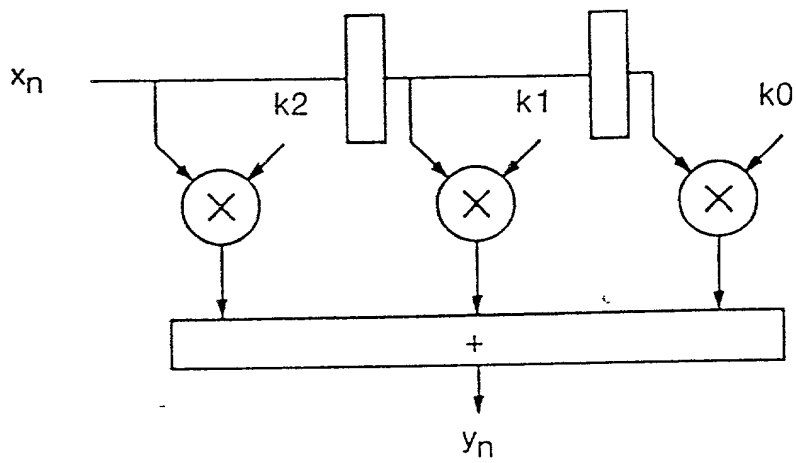


FIG. 167

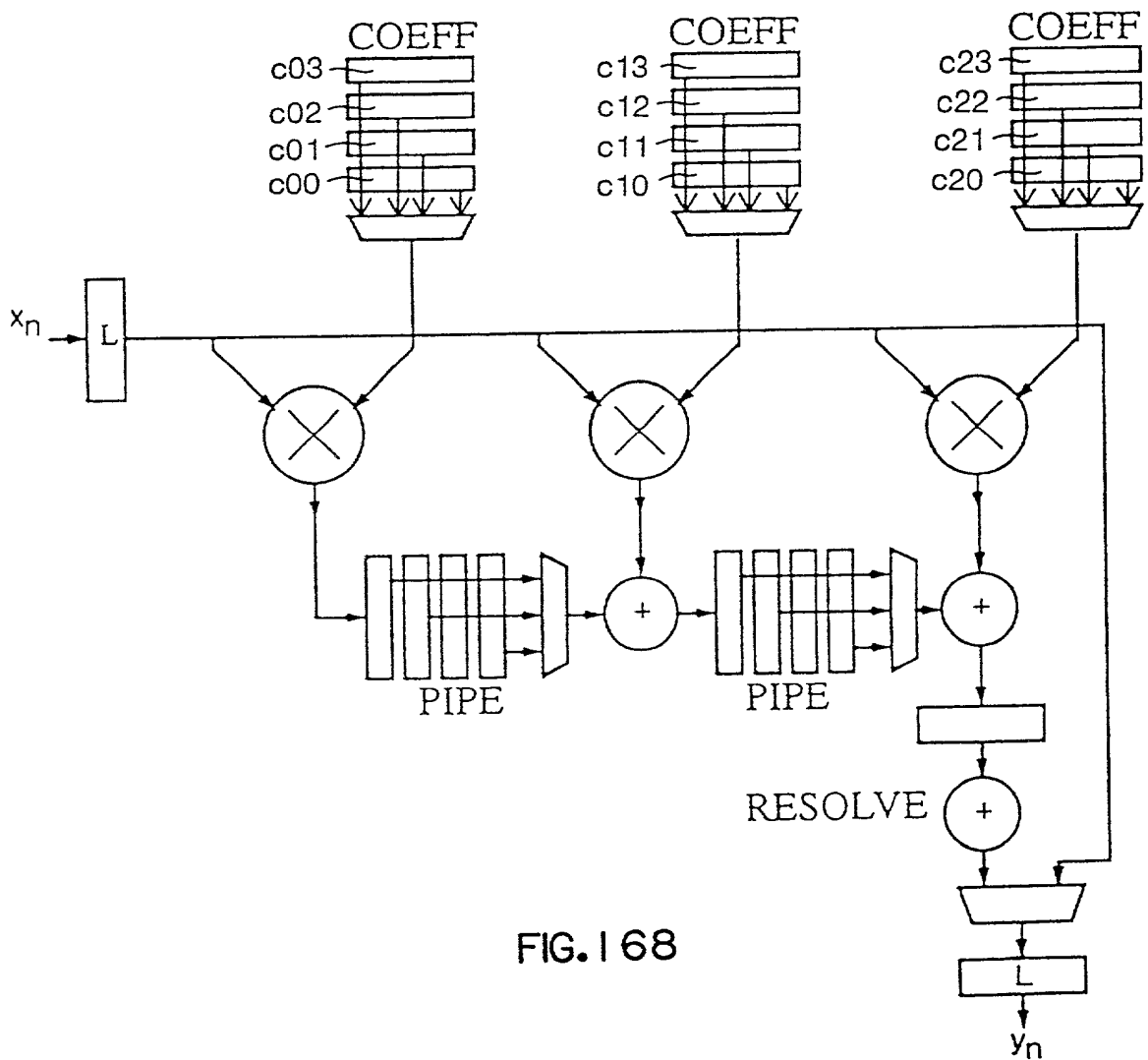


FIG. 168

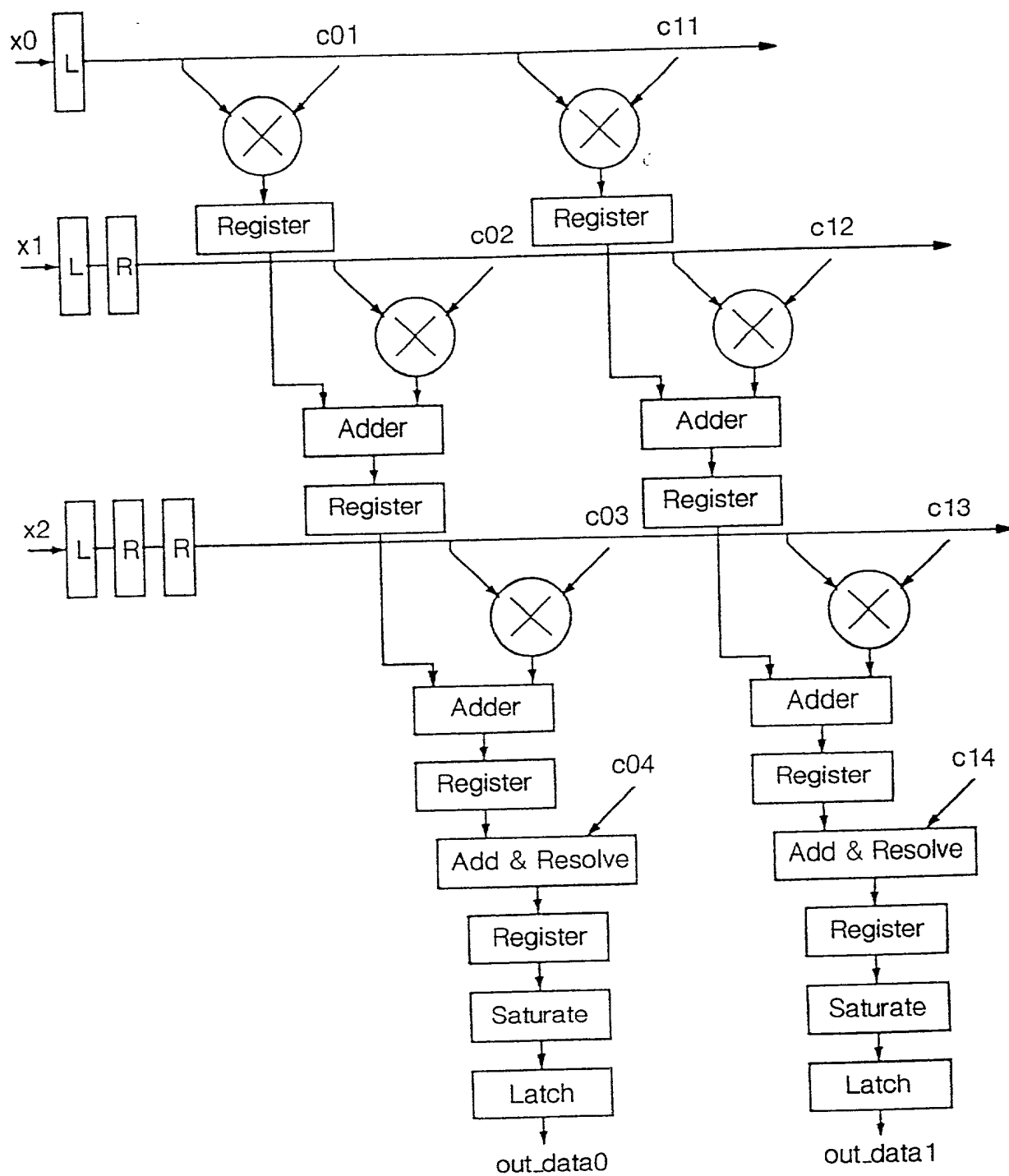


FIG. 169